KABARAK UNIVERSITY

UNIVERSITY EXAMINATIONS

2009/20010 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF COMPUTER SCIENCE

COURSE CODE: PHYS 120

COURSE TITLE: BASIC ELECTRONICS

STREAM: Y1S2

DAY: WEDNESDAY

TIME: 9.00 – 11.00 A.M.

DATE: 11/08/2010

INSTRUCTIONS:
*Answer Question **ONE** and **ANY** other **TWO***

PLEASE TURNOVER

QUESTION 1 (30 MARKS)

(a) The table below is BJT data extracted form the semiconductor data sheet. Besides Product and Description, explain the meaning of all other parameters. [4 marks]

Product	Description	Channel Polarity	IC Max (A)	V(BR)CEO Min (V)	hFE Min	hFE Max	fT Min (MHz)	PTM Max (W)	Package
2N4401G	General Purpose Transistor NPN	NPN	0.6	40	100	300	250	0.625	TO-92

(b) Starting with a 2D crystal structure of pure silicon material, illustrate how a p-type semiconductor is formed. [3 marks]

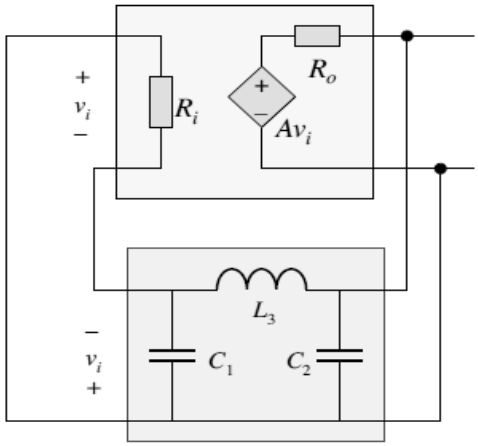
(c) Give any THREE differences between a JFET and a BJT. [3 marks]

(d) Draw the circuit of a Bridge rectifier and explain its operation [3 marks]

(e) Give the three regions of operations of the transistor and state the bias conditions of each. [6 marks]

(f) (i) State the conditions for sustained oscillations to occur in a feedback circuit. [2 marks]

(ii) The circuit below is an oscillator.

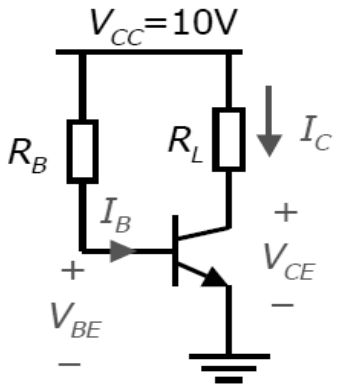


I. Name the oscillator type [1 mark]

II. Show that the resonance frequency is

$$\omega_0 = \frac{1}{\sqrt{L_3\left(\frac{C_1 C_2}{C_1 + C_2}\right)}}: \quad \text{[4 marks]}$$

g) Suppose, for the circuit below, we want the following biasing condition: I_C = 10 mA and V_{CE} = 5 V. Find R_B and R_L. [4 marks]



Transistor:
β = 100

QUESTION 2 (20 MARKS)

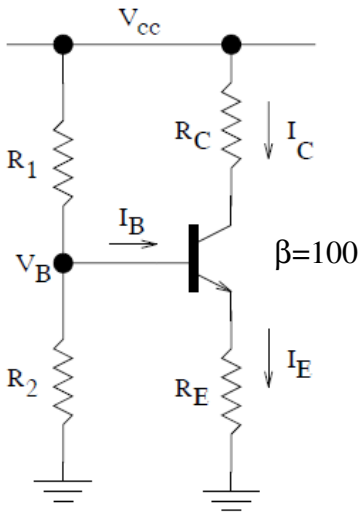
a) i) Sketch typical i/v characteristics of a transistor connected in common collector mode. [2 marks]

ii) State why the common collector mode is not popular in high gain amplifiers. [1 mark]

b) i) Define transistor biasing [1 mark]

ii) The circuit below shows an amplifier circuit where R_1=100 kΩ, R_2=20 kΩ, R_C=4 kΩ, R_E=500 Ω, V_{CC}=15 V and V_{BE}=0.6V.

.



I. Name the biasing method used [1 mark]

II. Show that

$$I_C \approx \frac{V_{BB} - V_{BE}}{R_E}$$

Hence, find all the three currents indicated on the circuit. [11 marks]

c). i) Draw a structure of a depletion mode JFET. [1 mark]

ii) Describe how the gate voltage controls the drain current in a JFET.[3 marks]

QUESTION 3 (20 MARKS)

a) Draw a black box representation of an amplifier with feedback, and use the diagram to show that the closed loop gain of an amplifier employing negative feedback is of the form

$A_0 = \frac{A}{1 + A\beta}$ where A is the open loop gain and β, the feedback factor.[6 marks]

b) Derive the expression for the input and output impedance of a series-shunt feedback amplifier. [6 marks]

c) Describe the following advantages of negative feedback amplifier

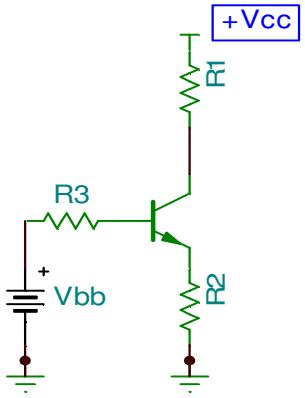
i) Minimization of gain distortion [4 marks]

ii) Bandwidth extension [4 marks]

QUESTION 4 (20 MARKS)

a) With the aid of a well labelled charge carrier flow diagram, derive the fundamental BJT relations. [8 marks]

b) For the circuit shown below, R_1= 4kΩ, R_3= 200kΩ, R2 = 500 Ω, β =100, V_{BE} = 0.7 V, V_{bb}= 5V and V_{CC} = 12 V.



i) Find the transistor currents I_B, I_C and I_E. [6 marks]

ii) Determine V_{CB} [3 marks]

iii) Draw the load-line and estimate the Q point [3 marks]