

KABARAK



UNIVERSITY

UNIVERSITY EXAMINATIONS

2008/2009 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF EDUCATION

SCIENCE

COURSE CODE: PHYS 420

COURSE TITLE: DIGITAL ELECTRONICS

STREAM: SESSION VIII

DAY: FRIDAY

TIME: 9.00 – 11.00 A.M.

DATE: 13/08/2010

INSTRUCTIONS:

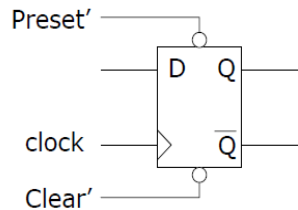
*Answer Question **ONE** and ANY other **TWO***

PLEASE TURN OVER

QUESTION 1 (30 MARKS)

- a) Explain the following logics
- i) Sequential logic (2 marks)
 - ii) Combinational logic (2 marks)

- b) Consider a data latch below:

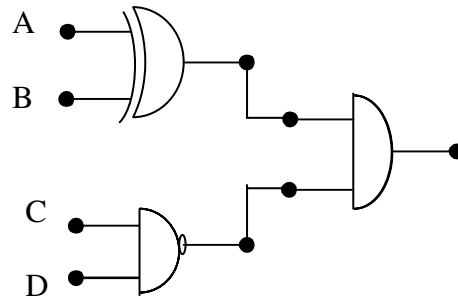


State the status of Q if

- i) $\text{Preset}'=0$ (1 mark)
 - ii) $\text{Clear}'=0$ (1 mark)
- c) State ANY two common uses of a register. (2 marks)
- d) i) Draw a diagram of a series in series out shift register employing four D latches. (4 marks)
- ii) Complete the table below for a shift register. (3 marks)

	In	Q ₁	Q ₂	Q ₃	Q ₄
t ₀	1				
t ₁	0	1			
t ₂	1		1		
t ₃	1	1		1	
t ₄	0	1	1		1
t ₅	0		1	1	

- f) Simplify the following expressions and draw the simplified logic circuit.
- i) $Y = \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D}$ (3 marks)
 - ii) $Y = \overline{(\overline{A} + C)} \cdot (B + \overline{D})$ (3 marks)
- g) Determine the output of the following logic circuits:

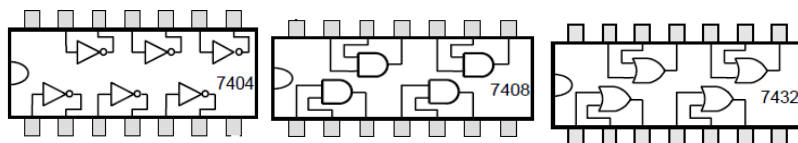


(4 marks)

- h) i) State the function of a MUX. (3 marks)
- ii) Draw a functional diagram of a 2-input MUX and deduce its output expression. (2 marks)
- iii) List two applications of a MUX (3 marks)

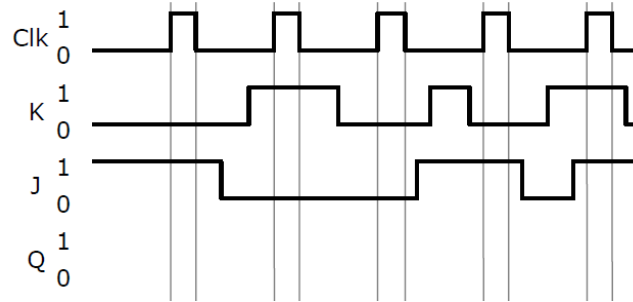
QUESTION 2 (20 MARKS)

- a) List TWO problems encountered with asynchronous counters (2 marks)
- b) List THREE differences between the asynchronous and synchronous counters. (3 marks)
- c) Draw a synchronous counter and explain its operation. (10 marks)
- d) Connect the chips provided below to implement $f = ab + b'c$ given pin 7 and 14 on each IC represent GND and $+V_{DD}$ respectively. (5 marks)



QUESTION 3 (20 MARKS)

- a) Given the numbers, decimal 227 and binary 1101101, convert both numbers to decimal, binary, hexadecimal and BCD equivalents where applicable. (8 marks)
- b) i) With the use of logic gates, draw a logic circuit of a JK flip flop. (3 marks)
- ii) Present the truth table of a JK flip flop. (5 marks)
- iii) Complete the following timing diagram of a NGT JK latch (3 marks)



- iv) State one advantage of JK over SR latch (1 mark)

QUESTION 4 (20 MARKS)

- a) Design a counter that counts from 0 to 9 using JK flip-flops that respond to NGT of the clock. Use additional logic to generate an output Z which activates an LED when a count of 5 or 7 is attained. (8 marks)
- b) i) Draw a block diagram of a full adder. (2 marks)
- ii) Give the truth table of the full adder using three inputs A, B and Cin (Carry-in) and the outputs Sum and carry-out. (4 marks)
- iii) Derive the expressions for sum and carry-out based on the truth table; hence draw a logic diagram for the full adder. (6 marks)