KABARAK UNIVERSITY

UNIVERSITY EXAMINATIONS

2009/2010 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF SCIENCE IN EDUCATION SCIENCE

COURSE CODE: PHYS 420

COURSE TITLE: DIGITAL ELECTRONICS

STREAM: SESSION VII & VIII

DAY: SATURDAY

TIME: 2.00 – 4.00 P.M.

DATE: 28/11/2009

INSTRUCTIONS:

ANSWER QUESTION **ONE** AND ANY OTHER **TWO** QUESTIONS.

PLEASE TURN OVER

QUESTION 1 (24 marks)

(a) Using only two-input NOR gates, show how a NAND gate can be made. (2marks)

(b) The circuits in fig. 1 are a D-latch and a D-flip-flop. Complete the timing diagram by drawing the waveforms of X and Y assuming that they are both low initially. (2marks)

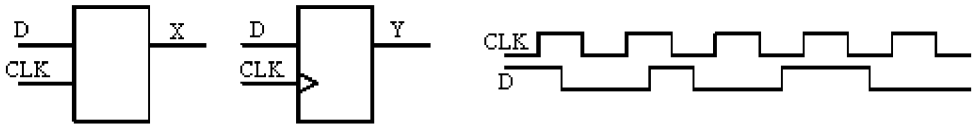


Fig. 1

(c) Given a logic function

$f = A.\overline{B}.C.\overline{D} + A.D + \overline{B}.\overline{C}.\overline{D} + \overline{A}.B.\ C.\overline{D} + \overline{A}.\overline{B}.D$

(i) Draw a Karnaugh map for f and write simplified function of f (3marks)

(ii) Design a NAND-only circuit to implement f. (2marks)

(iii) Design a NOR-only circuit to implement f. (2marks

(d)

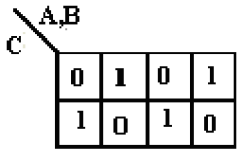
(i) Determine the maximum conversion time of an 8-bit ADC with a 2-MHz clock, if the ADC is of a staircase ramp type. (1mark)

(ii) Determine the percentage resolution of a 12-bit BCD DAC. (1mark)

(e)

i. Represent the function as a sum of product form from the pattern in a Karnaugh map below. (1 mark)

ii. Using Boolean algebra to simplify the logic expression in (i) and give the name of the gate. (1 mark)



(f) Differentiate between Combinational and sequential circuits (3 marks)

(g) Describe how a 2-to-1 MUX functions (6 marks)

QUESTION 2 (12 marks)

(a) If the 3-bit binary number *A B C* represents the digits 0 to 7:

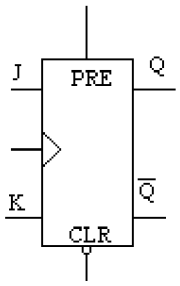
(i) Make a truth table for *A*, *B*, *C* and *Q*, where *Q* is true only when an odd number of bits are true in the number.

(ii) Write a statement in Boolean algebra for *Q*.

(iii) Convert this equation to one that can be mechanized using only two XOR gates. Draw the resulting circuit.

(b) Show how gated-SR flip-flop can be modified to operate as a D flip-flop and draw the truth table for D flip-flop. (2marks)

(c) Design a modulo-7 asynchronous counter using JK flip-flops and sketch the counter circuit. The JK flip-flop is as shown below. (3marks)



(d) Modify the counter circuit in (c) above, so that the counter can be used as an electronic dice, i.e. counting, 1, 2, …. 6 rather than 0, 1, 2….6. (2marks)

QUESTION 3 (12 marks)

(a) With show of diagrams explain how adder-subtractor functions (10 marks)

(b) Differentiate between asynchronous and synchronous systems. (2 marks)

QUESTION 4 (12 marks)

With show of diagrams explain how XOR-gates can be used as :

i. A controlled inverter. (4 marks)

ii. A parity generator and checker. (8 marks)

QUESTION 5 (12 marks)

(a) Show how four D type flip-flops can be connected to form a shift register where data be rotated in, and explain how it functions. (6marks)

(b) A 3-bit binary number is represented as A_2 A_1 A_0 , where A_0 is the LSB. Design a logic circuit which will produce a HIGH output whenever the binary number is either 1, 2, 4 or 7. Impliment the circuit using :

(i) a 1 to 8 MUX . (3marks)

(ii) a 1 to 4 MUX. (3marks)

QUESTION 06 (12 marks)

With show of diagrams explain how a full adder can be developed out of two half-adders. (12 marks)

(a) Why is the above scheme impractical for implementing a 12-bit D/A converter circuit? (1mark)

(b) Why is a sample-and-hold amplifier usually used with an A/D converter? (3mark)