KABARAK UNIVERSITY

UNIVERSITY EXAMINATIONS

2010/2011 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF SCIENCE IN TELECOMMUNICATIONS

COURSE CODE: TLCM 221

COURSE TITLE: DIGITAL ELECTRONICS AND MICROPROCESSOR CONTROL

STREAM: Y2S2

DAY: TUESDAY

TIME: 2.00 – 5.00 P.M

DATE: 14/12/2010

INSTRUCTIONS

- *Answer Question **ONE** and any other **THREE** Questions. Question One carries **20marks** while each of the other THREE Questions carry **10marks**.*
- *The **8085** Instruction set is appended.*

PLEASE TURN OVER

QUESTION 1 (20 marks)

a) i) Perform the following arithmetic

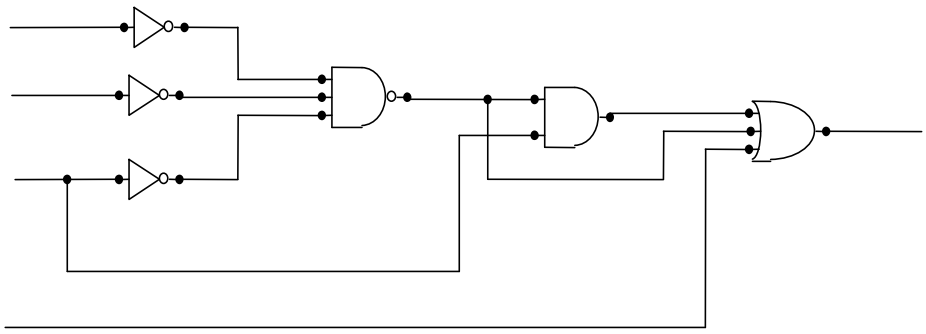
I) CDFH + ABCH (1mk)

II) 00001000 – 00000011 (1mk)

ii) Convert $(3.625)_{10}$ into binary (1mk)

b) i) State De-Morgan's theorem of two variables (1mk)

ii) Consider the given logic circuit



If the inputs are A, B, C and D in that order from top to bottom and the output is Y;

I) obtained the unsimplified output logic expression for the above circuit (2mks)

II) Using De-Morgan's and Boolean theorem's, simplify the output logic expression in (I) (2mks)

III) Draw a logic circuit of the simplified function in (II) (1mk)

c) i) What is a logic gate? (1mk)

ii) Show using diagrams how you can use a NAND gate to implement an AND function and an OR function (2mks)

d) State two differences between a microprocessor and a microcontroller (2mks)

e) Write down an assembly language program of adding two numbers 234H and 566H using 8085 instruction set (2mks)

g) Differentiate between the following

i). Instruction set and addressing modes (2mks)

ii). Register addressing mode and register indirect addressing mode with respect to 8085 microprocessor. Write a short 8085 instruction example to illustrate the difference between the two addressing. (2mks)

QUESTION 2 (10 marks)

a) i) Draw a logic symbol of a NOR gate (1mk)

ii) Manipulate the given logic function into a form which can be implemented using NOR gates only (2mks)

$$Y = \bar{A}B\bar{C} + AC + \bar{B}$$

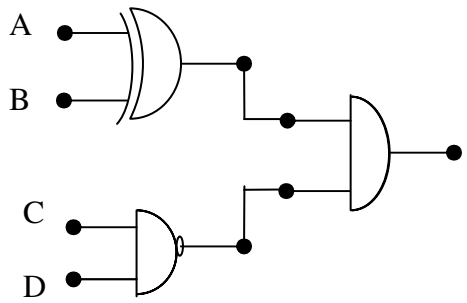
iii) Draw the logic diagram of the resulting manipulated function in (ii) above (1mk)

b) Simplify the following logic expressions and draw the logic circuits for the simplified functions.

i) $W = X.Y + \bar{X}.Y + \bar{X}.\bar{Y}$ (2mks)

ii) $Y = \overline{(\bar{A} + C) \cdot (B + \bar{D})}$ (2mks)

f) Determine the output of the following logic circuits:



(2mks)

QUESTION 3 (10 marks)

a) i) Outline the components required for the design of a microprocessor-based system. (2mks)

ii) Give in block diagram how the components in (ii) are organized to form the system. (2mks)

c) What is stack? How is it specified? (1mk)

d) Consider the following assembly language program of a microprocessor-based system using the 8255 PPI.

```
        MVI A, 80H
        OUT 03H
START:  MVI A, AAH
        OUT 00H
        OUT 01H
        OUT 02H
        CALL SUBTASK
        MVI A, 55H
        OUT 00H
        OUT 01H
        OUT 02H
        CALL SUBTASK
        JMP START
SUBTASK: LXI D, FFDFH
AGAIN:  DCX D
        MOV A, E
        ORA D
        JNZ AGAIN
        RET
```

i.) Suggest what the first two instruction are doing (1mk)

ii.) Name the labels used in this program and state their importance (1mk)

iii.) Suggest what the whole program is doing (1mk)

iv.) Hand assembles the above program showing only two columns of address and memory contents in hex codes. Assume the first memory location is 489EH. (2mk)

QUESTION 4 (10 marks)

a) i) State and explain two types of interfaces. (1mk)
ii) State and explain two features that need to be considered when selecting an interface circuit (1mk)

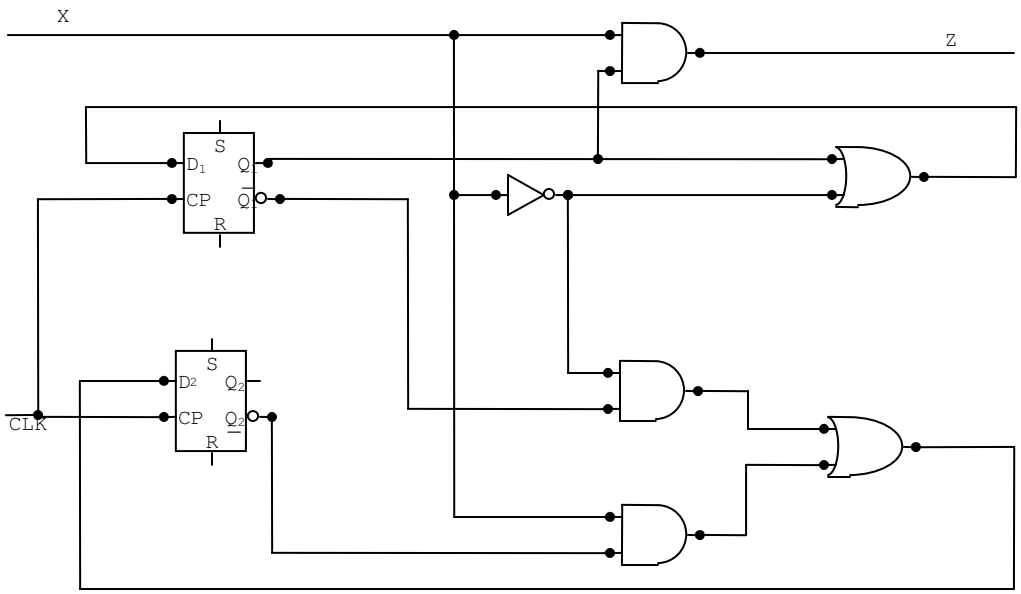
b) i) State and explain two modes of operation of 8255 PPI (1mk)
ii) Present the control word format of 8255 PPI (2mks)

c) A microprocessor-based system uses the 8255 PPI as its I/O device. If this system is to be used to read bit pattern from port B and output the same to port A and Port C continuously and endlessly;
i) Write an assembly language program to perform this operation using appropriate 8085 instruction set. Assume that the first memory location is 78EFH and use a delay constant of FDEFH between the outputs in register pair BC. (3mks)
ii) State the memory address of the last byte of the instruction in (i) above (1mk)
iii) State two advantages of using mnemonics as opposed to binary values or hex codes. (1mks)

QUESTION 5 (10 marks)

a) Define the following terms as used with sequential circuits (2mks)
i). State
ii). State diagrams
iii). State tables
iv). Clock width

b) Consider the following sequential circuit



The circuit has one input X, one output Z and two state variables Q_1 and Q_2

i). Write the Boolean expressions which can be used to determine the behavior of the circuit (2mks)

ii). From the Boolean expressions in (i), develop the state table for this circuit. Assume the circuit present state is 00 and input $X = 0$ (2mks)

iii). Use the state table to develop the state diagram for this circuit. (2mks)

c) Draw a programmable array which can give (2mks)

$$W_1 = \bar{A}.B\ ,\ W_2 = \bar{A}.\bar{B}\ ,\ W_3 = A\bar{B}\ ,\ W_4 = A.B$$

THE 8085 INSTRUCTION SET

CE	ACI	N	3D	DCR	A	7E	MOV	A,M
8F	ADC	A	05	DCR	B	47	MOV	B,A
88	ADC	B	0D	DCR	C	40	MOV	B,B
89	ADC	C	15	DCR	D	41	MOV	B,C
8A	ADC	D	1D	DCR	E	42	MOV	B,D
8B	ADC	E	25	DCR	H	43	MOV	B,E
8C	ADC	H	2D	DCR	L	44	MOV	B,H
8D	ADC	L	35	DCR	M	45	MOV	B,L
8E	ADC	M	0B	DCX	B	46	MOV	B,M
87	ADD	A	1B	DCX	D	4F	MOV	C,A
80	ADD	B	2B	DCX	H	48	MOV	C,B
81	ADD	C	3B	DCX	SP	49	MOV	C,C
82	ADD	D	F3	DI		4A	MOV	C,D
83	ADD	E	FB	EI		4B	MOV	C,E
84	ADD	H	76	HLT		4C	MOV	C,H
85	ADD	L	DB	IN	N	4D	MOV	C,L
86	ADD	M	3C	INR	A	4E	MOV	C,M
C6	ADI	N	04	INR	B	57	MOV	D,A
A7	ANA	A	0C	INR	C	50	MOV	D,B
A0	ANA	B	14	INR	D	51	MOV	D,C
A1	ANA	C	1C	INR	E	52	MOV	D,D
A2	ANA	D	24	INR	H	53	MOV	D,E
A3	ANA	E	2C	INR	L	54	MOV	D,H
A4	ANA	H	34	INR	M	55	MOV	D,L
A5	ANA	L	03	INX	B	56	MOV	D,M
A6	ANA	M	13	INX	D	5F	MOV	E,A
E6	ANI	N	23	INX	H	58	MOV	E,B
CD	CALL	NN	33	INX	SP	59	MOV	E,C
DC	CC	NN	DA	JC	NN	5A	MOV	E,D
FC	CM	NN	FA	JM	NN	5B	MOV	E,E
2F	CMA		C3	JMP	NN	5C	MOV	E,H
3F	CMC		D2	JNC	NN	5D	MOV	E,L
BF	CMP	A	C2	JNZ	NN	5E	MOV	E,M
B8	CMP	B	F2	JP	NN	67	MOV	H,A
B9	CMP	C	EA	JPE	NN	60	MOV	H,B
BA	CMP	D	E2	JPO	NN	61	MOV	H,C
BB	CMP	E	CA	JZ	NN	62	MOV	H,D
BC	CMP	H	3A	LDA	NN	63	MOV	H,E
BD	CMP	L	0A	LDAX	B	64	MOV	H,H
BE	CMP	M	1A	LDAX	D	65	MOV	H,L
D4	CNC	NN	2A	LHLD	NN	66	MOV	H,M
C4	CNZ	NN	01	LXI	B,NN	6F	MOV	L,A
F4	CP	NN	11	LXI	D,NN	68	MOV	L,B
EC	CPE	NN	21	LXI	H,NN	69	MOV	L,C
FE	CPI	N	31	LXI	SP,NN	6A	MOV	L,D
E4	CPO	NN	7F	MOV	A,A	6B	MOV	L,E
CC	CZ	NN	78	MOV	A,B	6C	MOV	L,H
27	DAA		79	MOV	A,C	6D	MOV	L,L
09	DAD	B	7A	MOV	A,D	6E	MOV	L,M
19	DAD	D	7B	MOV	A,E	77	MOV	M,A
29	DAD	H	7C	MOV	A,H	70	MOV	M,B
39	DAD	SP	7D	MOV	A,L	71	MOV	M,C
72	MOV	M,D	E5	PUSH	H	9D	SBB	L
73	MOV	M,E	F5	PUSH	PSW	9E	SBB	M

74	MOV	M,H	17	RAL		DE	SBI	N
75	MOV	M,L	1F	RAR		22	SHLD	NN
3E	MVI	A,N	D8	RC		30	SIM	
06	MVI	B,N	C9	RET		F9	SPHL	
0E	MVI	C,N	20	RIM		32	STA	NN
16	MVI	D,N	07	RLC		02	STAX	B
1E	MVI	E,N	F8	RM		12	STAX	D
26	MVI	H,NN	D0	RNC		37	STC	
2E	MVI	L,N	C0	RNZ		97	SUB	A
36	MVI	M,N	F0	RP		90	SUB	B
00	NOP		E8	RPE		91	SUB	C
B7	ORA	A	E0	RPO		92	SUB	D
B0	ORA	B	0F	RRC		93	SUB	E
B1	ORA	C	C7	RST	0	94	SUB	H
B2	ORA	D	CF	RST	1	95	SUB	L
B3	ORA	E	D7	RST	2	96	SUB	M
B4	ORA	H	DF	RST	3	D6	SUI	N
B5	ORA	L	E7	RST	4	EB	XCHG	
B6	ORA	M	EF	RST	5	AF	XRA	A
F6	ORI	N	F7	RST	6	A8	XRA	B
D3	OUT	N	FF	RST	7	A9	XRA	C
E9	PCHL		C8	RZ		AA	XRA	D
C1	POP	B	9F	SBB	A	AB	XRA	E
D1	POP	D	98	SBB	B	AC	XRA	H
E1	POP	H	99	SBB	C	AD	XRA	L
F1	POP	PSW	9A	SBB	D	AE	XRA	M
C5	PUSH	B	9B	SBB	E	EE	XRA	N
D5	PUSH	D	9C	SBB	H	E3	XTHL	