

KABARAK



UNIVERSITY

EXAMINATIONS

2008/2009 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF COMMERCE

COURSE CODE: COMP 451

**COURSE TITLE: MICROPROCESSOR BASED DESIGN
SYSTEMS**

STREAM: Y4S1

DAY: TUESDAY

TIME: 9.00 – 11.00 A.M.

DATE: 24/03/2009

INSTRUCTIONS:

**ATTEMPT QUESTION ONE AND ANY OTHER TWO
QUESTIONS**

QUESTION ONE CARRIES 30 MARKS AND THE REST 20 EACH

PLEASE TURN OVER

QUESTION ONE (20 MARKS)

- (a) A basic computer has a memory capacity of 8192 words, each word containing 32 bits.
- (i) List all the registers used in a block diagram format. (5 mks)
 - (ii) State the number of bits in each register. (5 mks)
 - (iii) In just one sentence, state the function of each register. (2.5 mks)
- (b) (i) The internal organization of a digital computer is best defined by specifying three parameters. Name them. (1.5 mks)
- (ii) On the basis of one of the parameters in (i), classify digital systems. (2 mks)
- (c) Distinguish between the following:
- (i) Operation, micro operation and macro operation. (1.5 mks)
 - (ii) Fetch, Indirect, execute and interrupt cycle (2 mks)
 - (iii). Mention the four types of registers in a memory stack unit and briefly in just one sentence explain the function of each. (2.5 mks)
- (d) An 8-bit computer has a register R. Determine the values of the status bits S, C, V and Z after each of the following instructions. The initial value of each register is hexadecimal number 72.
- (a) Add immediate operand E6 to R. (2 mks)
 - (b) Add immediate operand 2E to R. (2 mks)
 - (c) Exclusive-OR R with R. (2 mks)
 - (d) And immediate operand 8D to R. (2 mks)

QUESTION TWO (20 MARKS)

- (a) Write a program to evaluate the arithmetic statement
- (i). Using a general-register-type with two address format (4 mks)
 - (ii) Using a stack organized computer with zero-address operation instruction. (6 mks)
- (b) In a block diagram, show the organization of a stack organized CPU. (3 mks)

(c) Show the sequence of micro operations the implement the following stack Operations.

- (i) PUSH (4 mks)
- (ii) POP. (3 mks)

QUESTION THREE (20 MARKS)

(a) A memory unit has a capacity of 65,536 words of 25 bits each. It is used in conjunction with a general purpose computer. The instruction code is divided into four parts. An indirect mode bit, operation code, two bits that specify a processor register and an address part.

- (i) What is the maximum number of operations that can be inco operated in the computer if the instruction is stored in one memory word. (5 mks)
- (ii) Draw the instruction word format indicating the number of bits. (3 mks)
- (iii) How many bits are there in MBR, MAR, PC of the said memory capacity. (3 mks)

(b) A computer is available without a program counter (PC). Instead , all instructions contain three parts: an operation code, an address of an operand, and the address of the next instruction. The operation code consists of 6 bits and the computer has a memory capacity of 8192 words.

- (i) How many bits must be in the memory if the instruction is to be stored in one word? Show the instruction word format. (4 mks)
- (ii)What other register is needed in the control unit besides an OPR? (1 mk)
- (iii)List the micro operation for the fetch cycle of this computer. (4 mks)

QUESTION FOUR (20 MARKS)

- (a) Draw a block diagram of the control unit, clearly showing how timing and control signals are generated. (10 mks)
- (b) Show the sequence of micro operations that will implement the fetch cycle (5 mks)
- (c) Show the sequence of micro operations that will implement the interrupt cycle (5 mks)

QUESTION FIVE (20 MARKS)

(a) The increment and skip instruction is useful for address modification and counting the number of times a program loop is executed.

(i) Show the macro-statement for this instruction. (2 mks)

(ii) The sequence of micro-operations that implements operation. (4 mks)

(b) Draw a block diagram of an Intel 8080 microprocessor. (6 mks)

(c) An arithmetic circuit has two selection variables S_1 and S_0 . The arithmetic operations available in the unit are list below. Determine the circuit that must be in cooperated with a full-adder in each stage of the arithmetic unit (8 mks)

S_1	S_0	$C_1 = 0$	$C_1 = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A$	$F = A + 1$
1	0	$F = A + B$ complement	$F = A + B$ complement + 1