KABARAK UNIVERSITY

UNIVERSITY EXAMINATIONS

2008/2009 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCINCE

COURSE CODE: COMP 451

COURSE TITLE: MICROPROCESSOR – BASED DESIGN

STREAM: Y4S1

DAY: FRIDAY

TIME: 9.00 – 11.00 A.M.

DATE: 07/08/2009

INSTRUCTIONS:

1. Attempt question **one** and any other two questions.
2. Question one carries **30** marks and the rest **20** each.

PLEASE TURN OVER

QUESTION ONE (30 MARKS)

(a) A memory unit has a capacity of 65,535 words of 25 bits each. It is used in conjunction with a general purpose computer. The instruction code is divided into four parts. An indirect mode bit, operation code, two bits that specify a processor register and an address part.

(i) What is the maximum number of operations that can be incorporated in the computer if the instruction is stored in one memory word. (1mk)

(ii) Draw the instruction word format indicating the number of bits and the function of each part. (2mks)

(iii) How many bits are there in MBR, MAR and PC for the said memory capacity. (3 mks)

(b) (i) What is a control flow chart? (1 mk)

(ii) Name two types of blocks used in a low chart, clearly explaining the function of each of them. (4 mks)

(iii) Use a control flow chart to summarize the paths taken by the control unit during an execute cycle. (5 mks)

(c) Distinguish between the following:

(i) Operation, micro operation and a macro operation (1.5 mks)

(i) Fetch cycle, indirect cycle, execute cycle and interrupt cycles (2 mks)

(ii) Memory – reference, register – reference and input – output reference Instructions. (2.5 mks)

(d) An 8 – bit computer has a register R. Determine the values of the status bits S, C, Z and V after each of the following instructions. The initial values of each register R in each case is hexadecimal 72. The numbers below are also in hexadecimal:

(a) Add immediate operand C6 to R (2 mks)

(b) Add immediate operand IE to R (2 mks)

(c) Exclusive – OR R with R (2 mks)

(d) AND immediate operand 8D to R. (2 mks)

QUESTION TWO (20 MARKS)

(a) It is the function of the control unit to keep track of various cycles that occur during a Computer run. Draw a block diagram of the control unit showing various components

that are used in generation of various control functions. (7 mks)

(b) An instruction is read from memory during the fetch cycle. Show the register transfer relations that specify this process. (7 mks)

(c) The register transfer micro operation that specifies an interrupt cycle. (6 mks)

QUESTION THREE (20 MARKS)

(a) The increment and skip instruction is useful for address modification and counting the number of times a program loop is executed. Show

(i) The macro-statement of the instruction (2 mks)

(ii) The sequence of micro operation that implements the instruction. (6 mks)

(b) Distinguish between the following instructions, clearly stating the micro operations that implements them

(i) BUN: Branch unconditionally (6 mks)

(ii) BSA: Branch and save address. (6 mks)

QUESTION FOUR (20 MARKS)

(a) Draw a block diagram of an Intel 8080 microprocessor. (5 mks)

(b) From the table below, List

(i) List of the control functions. (8 mks)

(ii) List of the micro operations that execute these instructions. (7 mks)

Operation code	Symbolic function	Description
000	AC ← AC + M	ADD TO AC
001	If (AC > 0) Then PC ← m)	Branch If Ac is positive and non- zero
010	M ← M BR	Store in Ac

011	If (M =0), Then PC ← PC +1	Increment and skip if zero

QUESTION FIVE (TWENTY MARKS)

(a) Write the programs to evaluate the arithmetic statement

X = (A+B) * (C+D)

(i) Using a general-register –type computer with two-address instruction. (4 mks)

(ii) Using a stack organized CPU with zero-address operation instruction. (4 mks)

(b) In some details write and explain the sequence of micro operations that implements the following operations in a stack memory.

(a) Push operation (2 mks)

(b) Pop operation. (2 mks)

(c) An arithmetic circuit has two selection variables S_1 and S_0. The arithmetic operations available in the unit are listed below. Determine the circuit that must be in cooperated with a full adder in each stage of the arithmetic unit.

S_1	S_0	$C_1 = 0$	$C_1 = 1$	
0	0	F = A + B	F = A + B +1	
0	1	F = A	F = A + 1	
1	0	F = $\overline{B}$	F = $\overline{B}$ +1	
1	1	F = A + $\overline{B}$	F = A + $\overline{B}$ +1	(8 mks)