KABARAK UNIVERSITY

EXAMINATIONS

2009/2010 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF COMPUTER SCIENCE

COURSE CODE: **COMP 451**

COURSE TITLE: **MICROPROCESSOR – BASED DESIGN**

STREAM: **Y4S1**

DAY: **FRIDAY**

TIME: **9.00 – 11.00 A.M.**

DATE: **04/12/2009**

INSTRUCTIONS:

1. Attempt question **ONE** and any **OTHER TWO** questions.
2. Question one carries **30 MARKS** and the rest **20** each.

PLEASE TURN OVER

QUESTION ONE (30 MARKS)

(a) A computer is available without a program counter (PC). Instead, all instructions contain three parts: an operation code, an address of an operand, and the address of the next instruction. The operation code consists of 6 bits and the computer has a memory unit of 8192 words,

(i) How many bits must be in a memory word if an instruction is stored in one word? Show the instruction word format. (1.5marks)

(ii) What other register is needed in the control unit besides an operation register? (1mark)

(iii)List the micro-operations for the instruction fetch cycle of this computer. Use any register specified in part (ii). (1.5 marks)

(b) Distinguish between the following:

(i) Operation, micro operation and a macro operation (1.5 marks)

(ii) Fetch cycle, indirect cycle, execute cycle and interrupt cycles (2 marks)

(iii) Memory – reference, register – reference and input – output reference Instructions. (2.5 marks)

(c) (i) The organization of a digital computer is best defined by specifying three parameters. Name them. (1.5 marks)

(ii) On the basis of one of the parameters name in c (i), classify digital systems. (1 mark)

(iii) In basic computers, what do you understand by term 'stored program concept' (0.5 mark)

(d) (i) What is a control flow chart? (0.5 mark)

(ii) Name two types of blocks used in a low chart, clearly explaining the function of each of them. (3.5 marks)

(iii) Use a control flow chart to summarize the paths taken by the control unit during an execute cycle. (5 marks)

(iii) An 8 – bit computer has a register R. Determine the values of the status bits S, C, Z and V after each of the following instructions. The initial values of each register R in each case is hexadecimal 72. The numbers below are also in hexadecimal:

(a) Add immediate operand C6 to R (2 marks)

(b) SUB immediate operand 1E to R (2 marks)

(c) Exclusive – OR R with R (2 marks)

(d) NAND R to R. (2 marks)

QUESTION TWO (30 MARKS)

The micro-operation C_2t_3: F $\leftarrow$ 0 is assumed to be the last in an execute cycle

(a) Modify the above micro operation to account for the interrupt cycle. (12 marks)

(b) Write the micro operations that implements the above cycle. (8 mark)

QUESTION THREE (20 MARKS)

(a) The increment and skip instruction is useful for address modification and counting the number of times a program loop is executed. Show

(i) The macro-statement of the instruction (2 marks)

(ii) The sequence of micro operation that implements the instruction.(6 marks)

(b) Distinguish between the following instructions, clearly stating the micro operations that implements them

(i) BUN: Branch unconditionally (6 marks)

(ii) BSA: Branch and save address. (6 marks)

QUESTION FOUR (TWENTY MARKS)

The list of register transfer statements that change the contents of AC can be reduced to two micro-operations and two control functions:

X_1: AC $\leftarrow$ AC $\wedge$ MBR

X_2: EAC $\leftarrow$ AC + MBR

(a) Determine the control functions X_1, X_2, (4 marks)

(b) Write the micro operation for the above macro-operations (16 marks)

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QUESTION FIVE (TWENTY MARKS)

Write the programs to evaluate the arithmetic statement

X = (A+B) * (C+D)

(i) Using a general-register –type computer with two-address instruction. (4 marks)

(ii) Using a stack organized CPU with zero-address operation instruction. (4 marks)

(b) Draw a block diagram showing the organization of a memory stack. (2 marks)

(c) In some details write and explain the sequence of micro operations that implements the following operations in a stack memory.

(i) Push operation (5 marks)

(ii) Pop operation. (5 marks)