KABARAK UNIVERSITY

EXAMINATIONS

2008/2009 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF COMPUTER SCIENCE

COURSE CODE: **COMP 454**

COURSE TITLE: **MICROPROCESSOR – INTERFACE**

STREAM: **Y4S1**

DAY: **MONDAY**

TIME: **11.00 – 1.00 P.M.**

DATE: **15/12/2008**

INSTRUCTIONS:

1. Attempt questions **one** and any other two questions.
2. Question one carries **30** marks and the rest **20** each.

PLEASE TURN OVER

QUESTION ONE (30 MARKS)

(a) (i) Distinguish between peripherals and interface units. (2 mks)

(ii) When is a peripheral said to be connected on-line and off-line (2 mks)

(iii)Name the five basic categories of I/O interfaces. (2.5 mks)

(b) (i) Mention the five major differences that exists between the central computer and a peripheral (2.5 mks)

(ii) Mentioned the three modes of data transfer between the microprocessor and peripherals (1.5 mks)

(c) Distinguish between the following terms

(i) Vectored and non-vectored interrupts. (2 mks)

(ii) Soft ware and hardware establishment of priority of simultaneous Interrupts. (2 mks)

(iii) Serial priority and parallel interrupt. (2 mks)

(iv) Bit time and baud rate (1.5 mks)

(v) Serial and parallel modes of data transfer (1 mks)

(d) (i) There are four types of commands that an interface may receive when being addressed by the CPU. Name them. (2 mks)

(ii) Asynchronous communication interface is said to be 'double buffered'. Briefly in one sentence explain. (2 mks)

(iii) Direct memory access (DMA) interface is initialized by the CPU. The process of intialisation involves specifying four parameters. List them. (4 mks)

(e) In data transfer under program control, if the input-output device is connected to the microprocessor

(i) In memory-mapped I/O mode (1 mks)

(ii) In isolated mode (1 mks)

Show the instruction that may be used to transfer contents of AC to the I/O device in each of the above cases.

QUESTION TWO (TWENTY MARKS)

(a) Design a priority interrupt hard ware system together with its priority encoder truth table. (10 mks)

(b) Consider a computer without priority interrupt hardware. Any interrupt request results in storing the return address in memory location 749 and branching to location 750. Explain how a priority can be established by means of software means, clearly showing the programs that must reside in the memory for handling the interrupt system (10 mks)

QUESTION THREE (TWENTY MARKS)

Some computers use the configuration shown in Fig.1 for the daisy-chain priority interrupt where PI, PO and VAD have their usual meaning.

(a) Explain the how the system operates to provide a priority interrupt. (8 mks)

(b) Design a circuit diagram of one-stage in the chain. (12 mks)

QUESTION FOUR (TWENTY MARKS)

An interface has three hand shake line which is a part of a standard that defines a general purpose interface bus (GPIB). A source labeled data valid (*DAV*), each destination unit can generate a signal labeled request for data (RFD) and another destination line labeled data accepted (DAC). Each of these two control wires are tied together and applied to the source.

(a) Draw a block diagram showing the pertinent connection between the CPU and the peripheral (6 mks)

(b) Draw a timing diagram for the hand shaking. (3 mks)

(c) (i) Explain in some details the mode of transfer between the source and the destination unit (5 mks)

(ii) Derive a sequence - of- events flow chart for the transfer. (6 mks)

QUESTION FIVE (TWENTY MARKS)

A DMA unit receives characters of 8-bits from a peripheral device, packs four characters in 32-bit word, and the stores words of 32-bit word n the memory.

(a) Design a block diagram that defines a set of registers for the DMA unit, CPU and the memory unit and briefly explain the function of ach register. (4 mks)

(b) Draw a flow chart showing the sequence of events for the memory operations with direct memory access (DMA) (12 mks)

(c) During the interrupt cycle, show the sequence of micro operations performed by the CPU in a priority interrupt hardware. (4 mks)

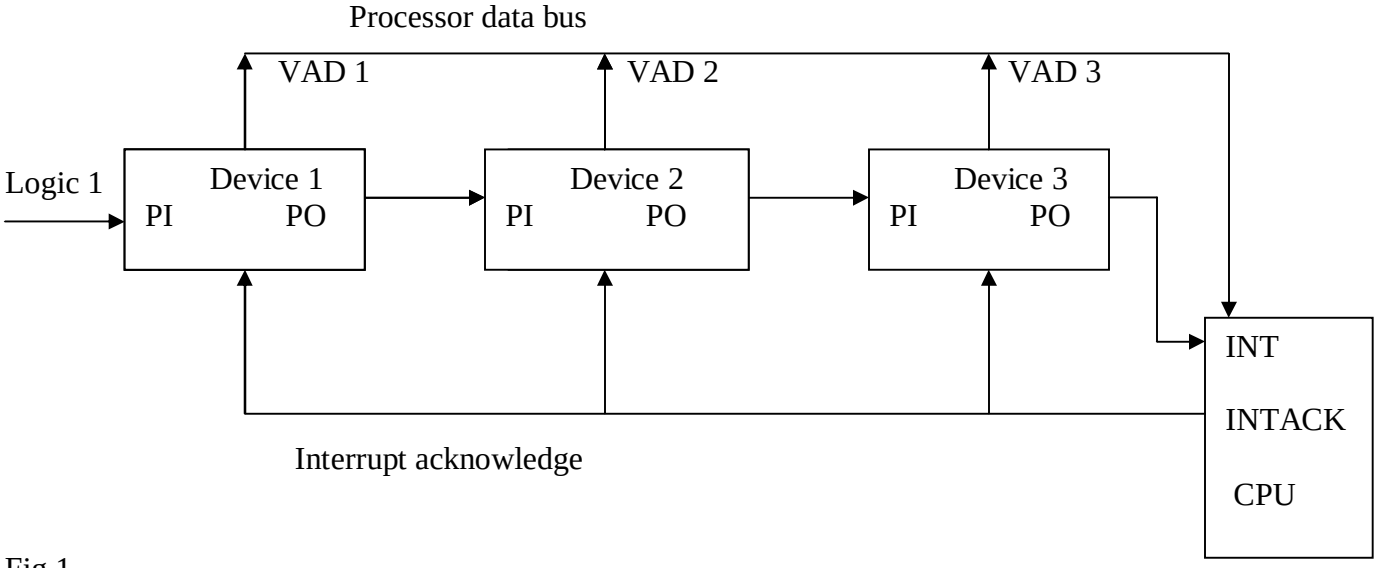

Fig.1.