KABARAK UNIVERSITY

UNIVERSITY EXAMINATIONS

2008/2009 ACADEMIC YEAR

FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCINCE

COURSE CODE: COMP 454

COURSE TITLE: MICROPROCESSOR – INTERFACE

STREAM: Y4S2

DAY: FRIDAY

TIME: 2.00 – 4.00 P.M.

DATE: 07/08/2009

INSTRUCTIONS:

1. Attempt question **one** and any other two questions.
2. Question one carries **30** marks and the rest **20** each.

PLEASE TURN OVER

QUESTION ONE (30 MARKS)

(a) (i) Distinguish between peripherals and interface units. (2mks)

(ii) When is a peripheral said to be connected on-line and off-line (2 mks)

(iii) Name the five basic categories of I/O interfaces. (2.5 mks)

(b) (i) Mention the five major differences that exists between the central computer and a peripheral (2.5 mks)

(ii) Mentioned the three modes of data transfer between the microprocessor and peripherals (1.5 mks)

(c) (i) Distinguish between the following terms

(ii) Vectored and non-vectored interrupts. (2 mks)

(iii) Soft ware and hardware establishment of priority of simultaneous Interrupts. (2 mks)

(iv) Serial priority and parallel interrupt. (2 mks)

(d) (i) In serial asynchronous data transfer, what are the four rules used by the receiver to detect the presence of a character? (4 mks)

(ii) How many characters per second can be transmitted over 1200-baud line of the following modes (assume a character code of eight bits)

(a) Synchronous serial transmission (1 mks)

(b) Asynchronous transmission with two stop bits (1.5 mks)

(c) Asynchronous transmission with one stop bit. (1.5 mks)

(d) Indicate whether the following constitute a test, control or data transfer commands

(i) Skip next instruction if the flag is set.

(ii) Seek a given record in the disk

(iii) Move paper tape to the next character position

(iv) Read status register (2.5 mks)

(e) What is the difference between an isolated I/O instruction and a memory –mapped I/O instructions. Give advantages and disadvantages in each case. (3 mks)

QUESTION TWO (TWENTY MARKS)

Some computers use the configuration shown in Fig.1 for the daisy-chain priority interrupt where PI, PO and VAD have their usual meaning.

(a) Explain the how the system operates to provide a priority interrupt. (8 mks)

(b) Design a circuit diagram of one-stage in the chain. (12 mks)

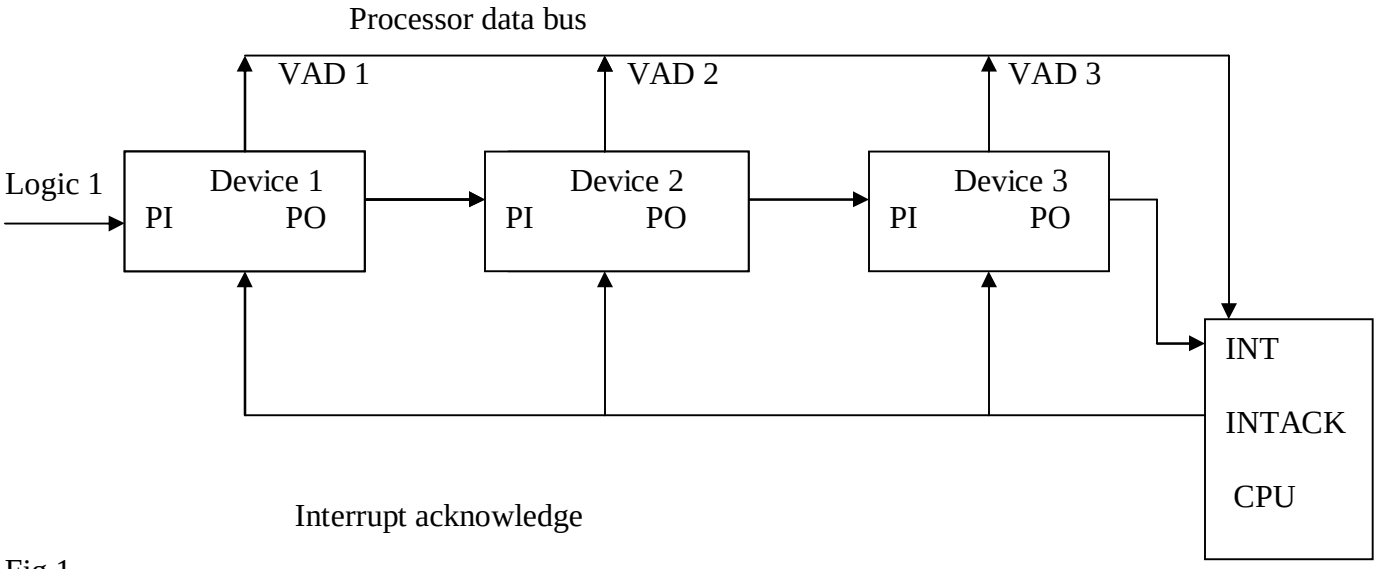

Fig.1.

QUESTION THREE (TWENTY MARKS)

An interface has three hand shake line which is a part of a standard that defines a general purpose interface bus (GPIB). A source labeled data valid ($\overline{DAV}$), each destination unit can generate a signal labeled request for data (RFD) and another destination line labeled data accepted (DAC). Each of these two control wires are tied together and applied to the source.

(a) Draw a block diagram showing the pertinent connection between the CPU and the peripheral (6 mks)

(b) Draw a timing diagram for the hand shaking. (3 mks)

(c) (i) Explain in some details the mode of transfer between the source and the destination unit (5 mks)

(ii) Derive a sequence - of- events flow chart for the transfer. (6 mks)

QUESTION FOUR (TWENTY MARKS)

A DMA unit receives characters of 8-bits from a peripheral device, packs four characters in 32-bit word, and stores words of 32-bit word in the memory.

(a) Design a block diagram that defines a set of registers for the DMA unit, CPU and the memory unit and briefly explain the function of each register. (4 mks)

(b) Draw a flow chart showing the sequence of events for the memory operations with direct memory access (DMA) (12 mks)

(c) During the interrupt cycle, show the sequence of micro operations performed by the CPU in a priority interrupt hardware. (4 mks)

QUESTION FIVE (TWENTY MARKS)

(a) Design a priority interrupt hardware system together with its priority encoder truth table. Explain its working. (11 mks)

(b) Consider a computer without priority interrupt hardware. Any interrupt request results in storing the return address in memory location 0 and branching to location 1. Explain how a priority can be established by software means. (5 mks)

(c) Information is inserted into a FIFO buffer at a rate m bytes per second. The information is deleted at a rate of n bytes per second. The maximum capacity of the buffer is k bytes.

(i) How long does it take for an empty buffer to fill when m> n? (1.5 mks)

(ii) How long does it take for a full buffer to empty when m< n? (1.5 mks)

(iii) Is the FIFO buffer needed if m = n? (1 mk)