KENYA METHODIST UNIVERSITY

END OF 2ND TRIMESTER 2010 EXAMINATIONS

SCHOOL : SCIENCE & TECHNOLOGY
DEPARTMENT : COMPUTER SCIENCE AND BUSINESS INFORMATION
UNIT CODE : CISY 301/BBIT 122
UNIT TITLE : COMPUTER ARCHITECTURE
TIME : 2 HOURS

Instructions: Attempt Question 1 and any other two questions.

Question 1 – 30 marks

a) Explain the following terms: (2 Mks)
   i. Computer Architecture
   ii. Computer Organization

b) Differentiate between the mechanical era computers and the electronic era computers. (2Mks)

c) Describe the von Neumann Architecture (4Mks)

d) List four levels of describing a computer (4Mks)

e) The most universally accepted method of describing or classifying computer systems is Flynn's Taxonomy developed in 1966. Using diagrams differentiate between following categories of computers
   i. SISD and MIMD (3Mks)
   ii. SIMD and MISD (3 Mks)

f) Briefly outline the general CPU instruction cycle and explain how an interrupt is handled by the instruction cycle. (5Mks)

g) Explain clearly the hard disks internal performance factors, namely, positioning and transfer latencies. Also explain the role of the onboard buffer. (5 Mks)

h) A computer's memory is organized into a hierarchy. State why this is necessary and with the help of a diagram explain the different levels in this hierarchy. (2 Mks)

SECTION B – Answer ANY TWO questions

Question 2 – 20 marks

a) Explain how the RAID hard disk technology is used for performance and reliability enhancement, particularly, explain the RAID levels 0 (striping) and 1 (mirroring). (5Mks)

b) A given microcomputer system is said to have 2 IDE channels referred to as the primary and secondary. How many hard disks can this system support? Explain your answer? (5Mks)

c) Explain the Coherency requirement in a cached memory system and briefly describe the write-through and write-back approaches respectively. (5Mks)

d) Distinguish between programmed I/O and interrupt driven I/O highlighting the advantages and any drawbacks. (5Mks)

Question 3 – 20 marks

a) Explain the mapping of an I/O module to the processor's I/O memory space. (5Mks)

b) Two sophisticated techniques for controlling I/O transfers are the use of DMA and the use of an I/O processor (IOP). Explain them as examples of the exploitation of *opportunities for parallelism* to maximize overall system performance. (5Mks)

c) In the context of system processor architecture explain the function of the control unit indicating what are its inputs and outputs and the dependency of outputs on inputs. (5Mks)

d) Explain the objective of the superscalar processor architecture. Also explain the negative effects that true data dependency has on the performance of a super scalar processor. (5Mks)

Question 4 – 20 marks

a) Explain what an instruction pipeline is and explain what impact branch instructions have on the effectiveness of the pipeline. (5Mks)

b) Write brief notes on the CISC and RISC processor architecture philosophies. (5Mks)

c) In the context of the CPU internal architecture describe the impact of the internal clock speed on performance. What establishes the upper limit on the clock speed? (5Mks)

d) One metric of computer system performance is the instruction throughput, i.e the number of instructions the system can execute per second. In this regard, briefly explain the influence of the CPU internal clock speed and the system bus clock speed on overall computer system performance. (5Mks)