EGERTON UNIVERSITY

UNIVERSITY EXAMINATIONS

NJORO CAMPUS

2005/2006 ACADEMIC YEAR

SECOND YEAR EXAMINATION FOR THE DEGREE IN BACHELOR OF SCIENCE IN INSTRUMENTATION & CONTROL ENGINEERING

ENGINEERING

ICEN 221: ELECTRONIC DEVICES

STREAM: Y2S1 BSc ICEN **TIME:** 2 HRS

DAY: MONDAY 3-5 P.M. **DATE:** 08.01.07

Instructions:

1. You should have the following for this examination
   - Answer book
   - scientific calculator
2. This paper contains 6 questions
3. Answer any FOUR of the SIX set
4. All questions carry equal marks

1. a) Define
   i) Semiconductor
   ii) Resistivity
   iii) Bulk resistance → $\frac{V - V_t}{I_F}$
   iv) Ohmic resistance
   v) Covalent bonding [2½ marks]

   b) i) Describe the difference between donor and acceptor impurities. [2 marks]

[2 marks]

ii) Describe the difference between majority and minority carriers. [2 marks]

c) i) State the diode equation and name all quantities involved. [5 marks]

ii) Using the equation in (i), derive the expression for the forward dynamic resistance (a:c) given by $rd = \frac{26mV}{I_D}$ [2½ marks]

Comment on the validity of this expression.

iii) Describe the 3 different resistance levels that characterize a diode depending on its forward bias conditions. [3 marks]

iv) Compare giving typical orders of magnitude all the resistances in (iii). [3 marks]

2. a) A silicon diode with a 0, 7V forward voltage drop at 25°C is to be operated with a constant forward current up to a temperature of 100°C. Calculate the diode V_F at 100°C. Also determine the junction dynamic resistance at 25°C and at 100°C if the forward current is 26mA. [3 marks]

b) Draw the circuit symbol and package for a zener diode indicating appropriately all relevant polarities, current and voltage. [3 marks]

c) For a zener diode show with the aid of a characteristic

i) Zener breakdown (V_z)
ii) Test current (I_{ZT})
iii) Minimum reverse current (I_{ZK})
iv) Maximum zener current(I_{ZM})
v) Dynamic impedance (Z_Z)

[5 marks]

d) A zener diode with $V_z = 4{,}3V$ has $Z_z = 22\Omega$ at $I_z = 20mA$. Calculate the upper and lower limits of V_Z when I_Z changes by $\pm 5mA$

e) Explain the 2 mechanisms that cause breakdown in a reverse-biased $\hat{p}n$ junction diode. [4 marks]

f) Define the Q point in a diode circuit; and explain how it is related to the diode characteristics and the dc load line. [3 marks]

Q3. a) Determine I, V_1, V_2 and V_0 for the series dc configuration in fig 3(a) [4 marks]

b) Determine the currents I_1, I_2 and I_{D_2} for the network of fig 3(b) [4 marks]

c) Determine the output wave form for the network in fig 3(c) and calculate the output dc level and the required PIV of each diode. [3 marks]

d) Assuming an ideal diode determine V_0 for the network in fig. 3(d) [3 marks]

e) i) For the network in fig 3(e), determine the range of R_L and I_l that will result in V_R, being maintained at IOV.

ii) Determine the maximum wattage rating of the diode. [6 marks]

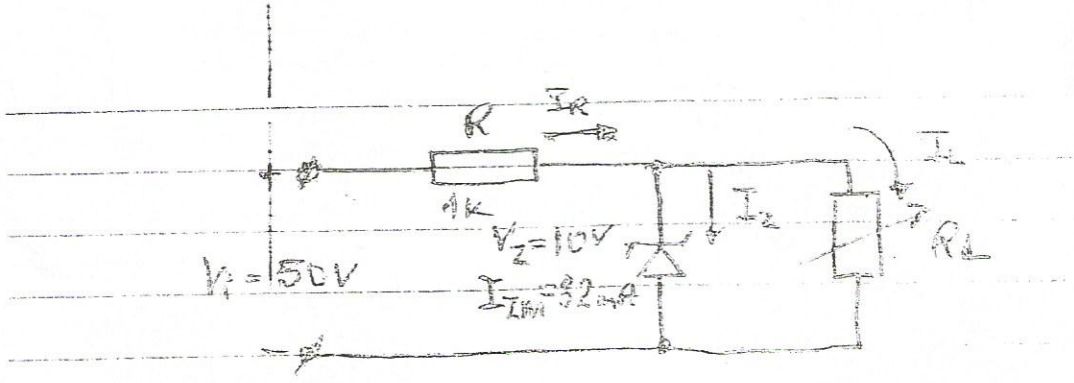


Fig 3(e)

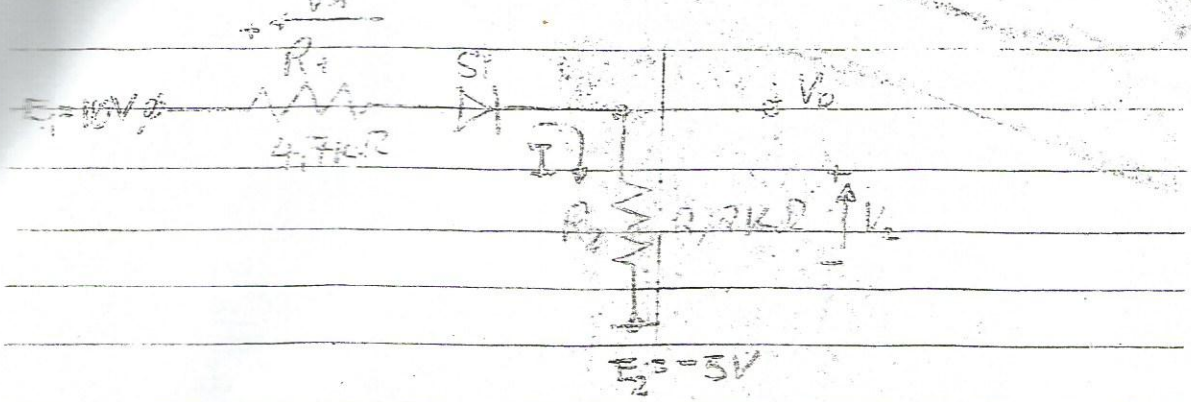


fig 3(a)

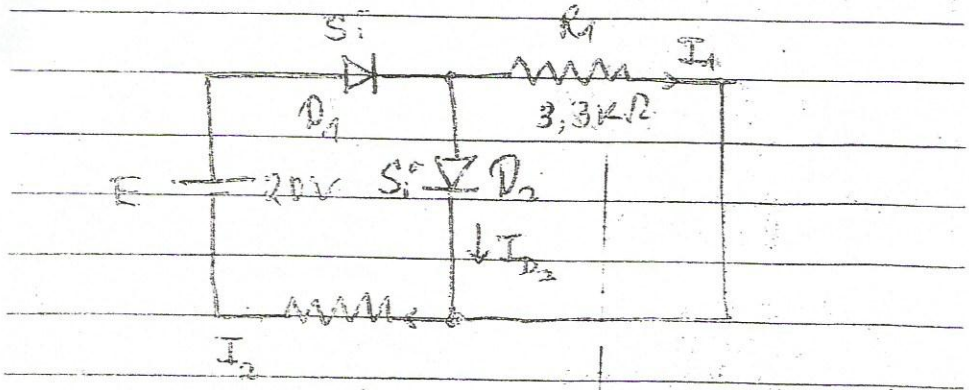


fig 3(b)

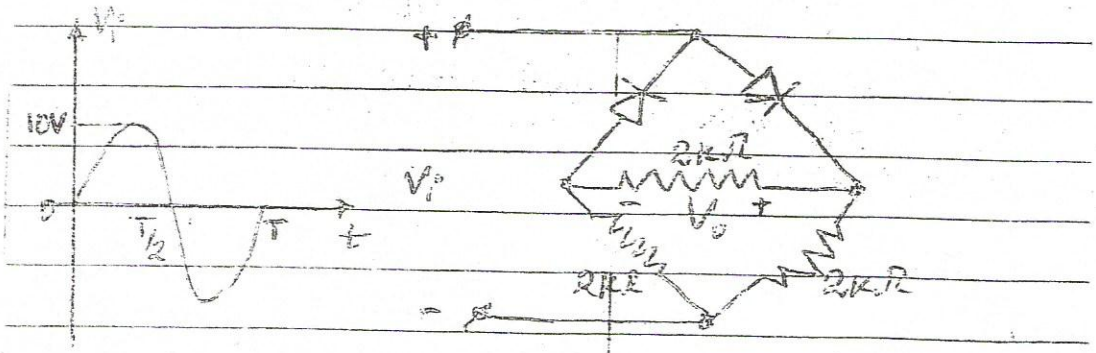
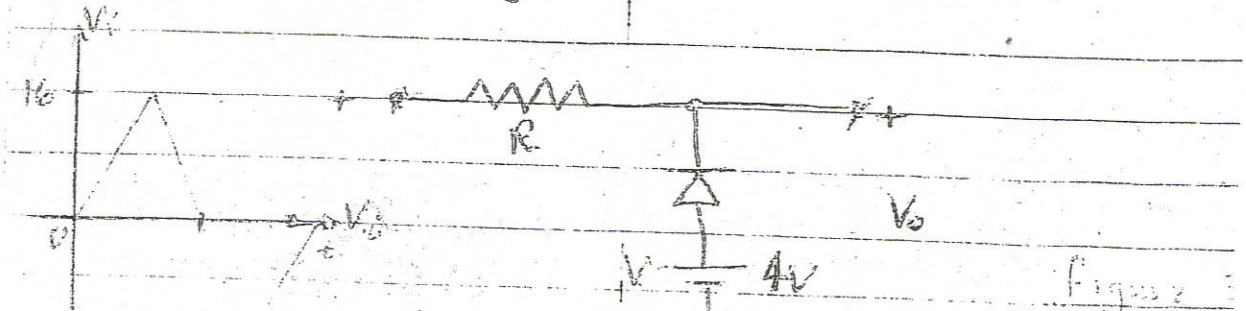


fig 3(c)



4. a) With the help of appropriate circuit diagrams explain procedures of how to obtain static output characteristic curves for the Common-Base, common Emitter and Common-collector configurations of a BJT. Draw for each case typical characteristic curves. [6 marks]

b) With the help of the output characteristics in (a) for the CE configuration, differentiate the 4 possible operating regions of a BJT. Briefly explain each operating region. [10 marks]

c) i) Explain the concept of a d.c load-line in a transistor circuit. [2 marks]

ii) How does β_{DC} vary with I_c and T (temperature) for a typical transistor.
Is β_{DC} the same for 2 different transistors, why? [2 marks]

5. a) What is transistor biasing and why is it important in electronic circuits. [2 marks]

b) Explain using appropriate circuit diagrams the following biasing circuits. Give practical hints on how to design such bias circuits.

i) Base Bias
ii) Collector-to-Base bias
iii) Voltage Divider Bias

In each case derive the appropriate expressions for the Q_{pt}. i.e. (I_c, V_{CE}) [12 marks]

c) For the circuits in figure 5 (a) and (b) determine the percentage change in Q pt for an increase in temperature from 25°C to 75°C. $\beta_{dc} = 100$ at 25°C and 150 at 75°C. [6 marks]

EGERTON UNIVERSITY

UNIVERSITY EXAMINATIONS

FIRST SEMESTER EXAMINATIONS

SECOND YEAR EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN INSTRUMENTATION AND CONTROL ENGINEERING

ICEN 221: ELECTRONIC DEVICES

STREAM: Y2S1 BSC ICEN **TIME:** 3 HRS

DAY: FRI 8.30-10.30AM. **DATE:** 01/04/2005

INSTRUCTIONS:

1. You should have the following for the examination.
   - Answer book
   - Scienctific calculator
2. This paper contains EIGHT questions
3. Attempt any FOUR questions
4. All questions carry equal marks.

1.(a) Explain the following:

(i) The difference between conductors and insulators?

(ii) The difference between semi conductors and conductors/insulators?

(iii) Why a semi conductor have fewer free electrons than a conductor?

(iv) The meaning of the term intrinsic and extrinsic semi conductor?

(v) How an n-type/p-type semi conductor formed?

(vi) How majority/minority carriers are produced. (6mrks)

(b) Explain with the aid of circuits, and characteristics how the following may be obtained:

(i) The diode forward characteristics.

(ii) The diode reverse characteristics. (6mrks)

(c)(i) A series circuit contains a power supply, Vps, a resistor R and a diode. If the diode is forward biased and the diode current is I_D, draw the circuit and obtain the expression for V_D, the voltage across the diode. State any assumption used.

(ii) If the supply voltage in (c)(i) is 6V and the resistance R is 1.5K, Calculate the silicon diode current and state any assumption(s) made.

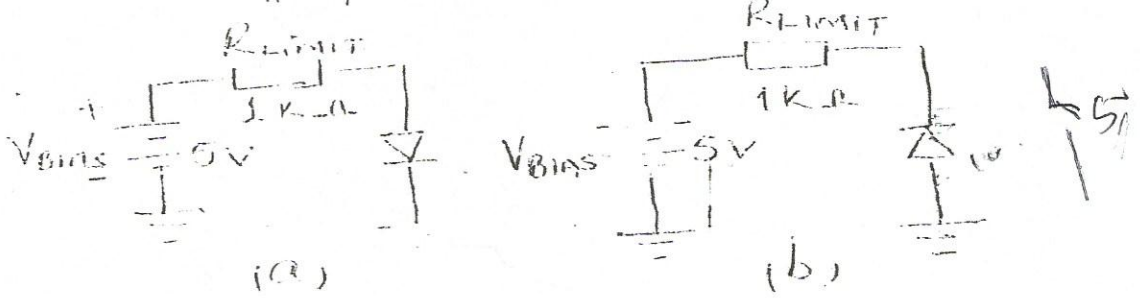
(iii) If the diode was germanium, calculate the current that would flow. (8mrks)

2(a) To more accurately model or represent a diode

(i) What 3 factors must be included (You may illustrate the answer using diagrams/circuits. (2mrks)

(ii) Determine the forward voltage and forward current for the diode in figure (a) for each of the 3 diode models (approximations). Also find voltage across limiting resistor in each case. Assume $r_d = 10\Omega$. (3mrks)

(iii) Determine the reverse voltage and reverse current for the diode in figure (b) for each of the diode models mentioned in (ii). Also find the voltage across the limiting resistor (R_{limit}) in each case. (3mrks)
Assume: $I_R = 1\ \mu A$



(b) A silicon pn junction diode at T=300^{0}K has a reverse – saturation current of $I_S = 10^{-14}$ A, V_T = 26mV at T= 300^0 K

(i) Determine the forward – bias diode current for;

V_D = 0.5V (ii) V_D = 0.6V (iii) V_D = 0.74 (1mrk)

(ii) Find the reverse – bias diode current for

V_D = -0.5V and (ii) V_D = -2V (1mrk)

where V_D = voltage applied across the diode.

(c) An alternating voltage is a applied to the circuits shown in Fig Q3(c). Explain with the aid of waveforms how the output voltage vo varies, (assume the diode forward voltage is 0.6 volts)

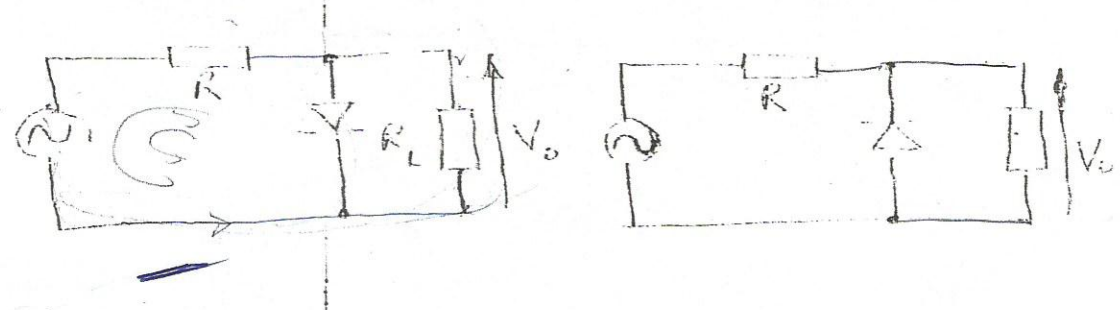


Fig. Q 3(c) (4mrks)

(d) Explain the operation of the circuits in Fq.Q3(c) and draw their truth tables. V1 and V2 could be zero or 5V and the forward diode voltage can be assumed to be 0.6V.

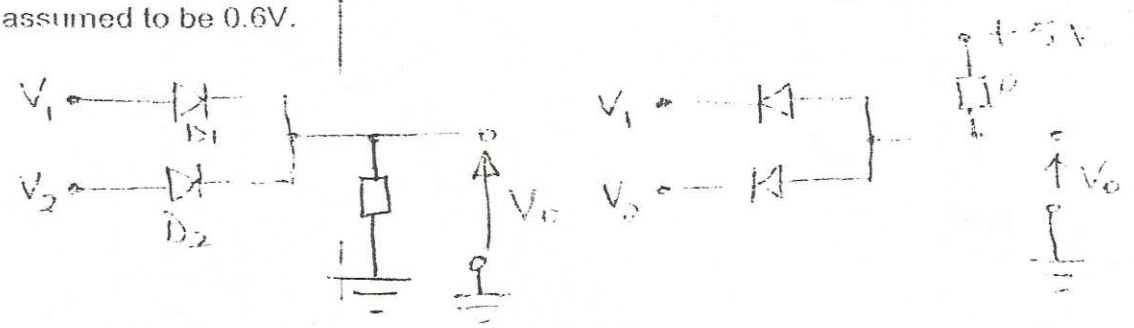


Fig.Q.3(d) (6mrks)

3(i) State what causes the ripple voltage on the output of a capacitor filter. (1 mark)

(ii) Explain what happens to the ripple voltage if the load resistance connected to a power supply is decreased. (1 mark)

(iii) Name one advantage of an LC filter over capacitor filter. (3mrks)

(b) A 10:1 step-down transformer has its secondary connected to a diode bridge rectifier and the rectifier output is applied to a C-R filter. The output is measured across the resistor R. If the transformer primary is connected to a 115V rms 60Hz supply and C and R are 50μF and 2.2KΩ respectively; draw the circuit and calculate the percentage ripple. Assume the diode forward voltage to be 0.6V. (6mrks)

(c) Derive the expressions for the average or D.C. voltage , Vdc, when a sinusoidal voltage with a maximum value Vm is applied to the following rectifiers:

(i) half-wave
(ii) full-wave

Calculate the average value if the applied voltage has an rms value of 12V. (9mrks)

4(i) With the help of appropriate circuit diagrams explain how to obtain static collector characteristic curves for the common-base and common-emitter configuration of a BJT. Draw the expected curves for both cases. (4mrks)

(ii) With the help of the collector characteristics curves mentioned in (i) for the CE configuration differentiate the 4 possible operating regions of BJT transistor (dependent on bias conditions). Briefly explain each bias condition/operating region. [12 marks]

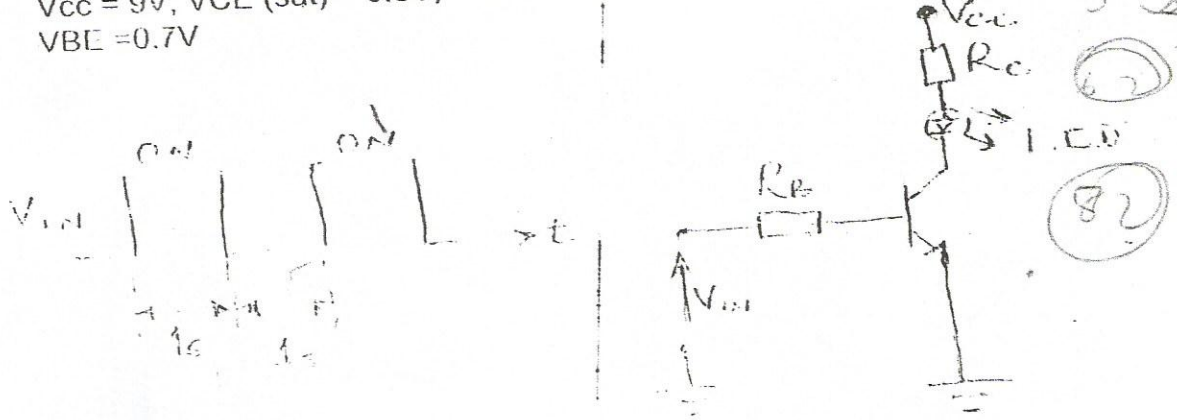
(iii) Explain why collector current increases slightly as the collector –emitter voltage increases in the active region of transistor bias in the common emitter (CE) configuration. (2mrks)

(iv) Explain the concept of a load-line and its application in transistor circuits. (2mrks)

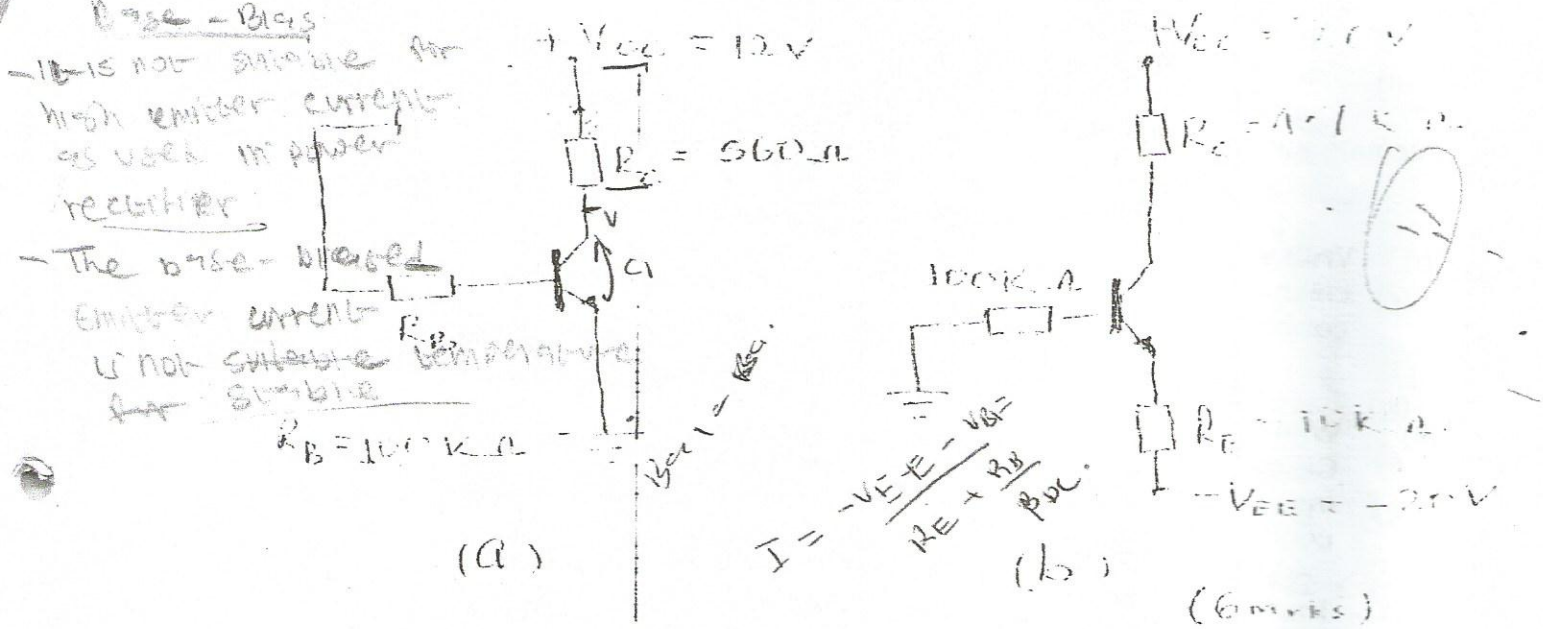
(v) A certain transistor has a (pp(max)) i.e maximum power dissipation rating of 4W at 25°C. The derating factor is 5m W/°C. What is the rating at a temperature of 70°C. (2mrks)

5(i) The LED in the figure requires 30 mA to emit a sufficient level of light. Therefore the collector current should be approximately 30mA. For the following circuit values determine the amplitude of the square wave input voltage necessary to make sure that the transistor saturates. Use double the minimum value of base currents as a safety margin to ensure saturation. (3mrks)

Vcc = 9V, VCE (sat) = 0.3V, Rc = 270Ω , R_B = 3.3KΩ, β_{DC} = 50, VBE =0.7V



(ii) For the circuit (a) and (b) determine the percentage change in Q – point values (Ic, VCE) of circuit is subjected to an increase in temperature from 25°C to 75°C, where β_{DC} = 100 at 25°C and 150 at 75° C.



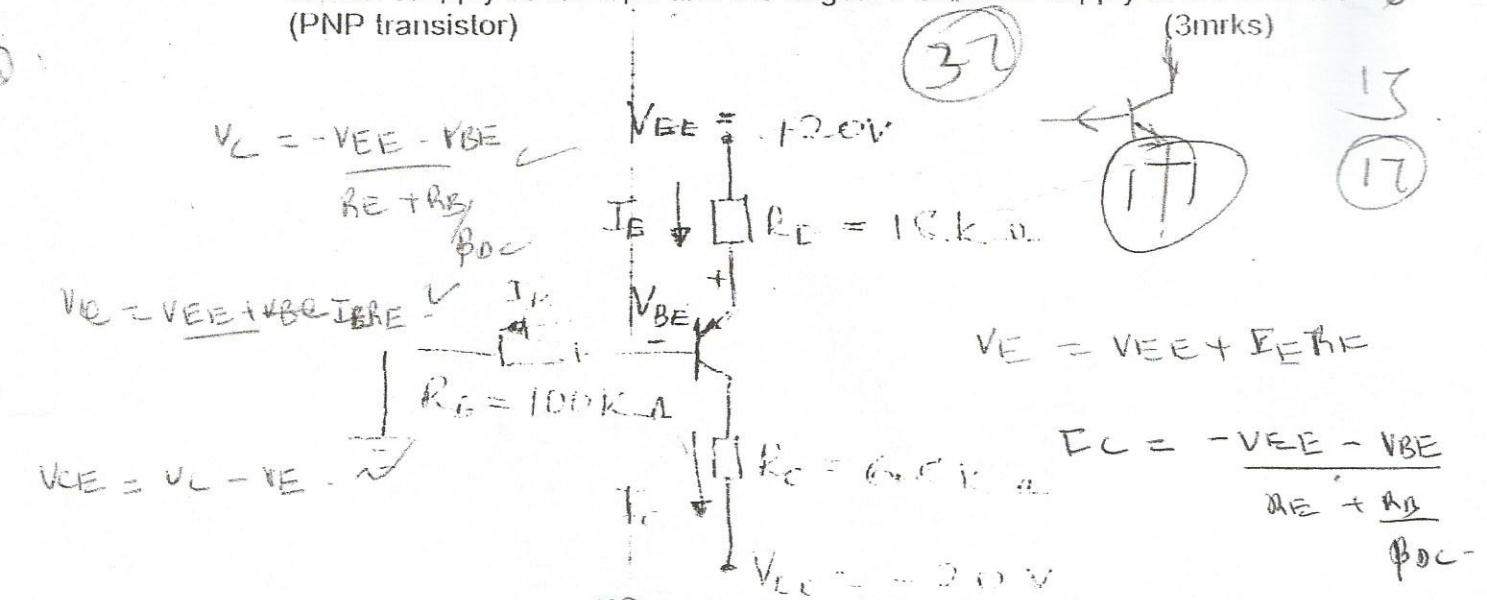
(6mrks)

(iii) What kind of bias circuits are illustrated in (ii), what is the advantage of one type over the other.

What is the main disadvantage of emitter bias? Give 2 other examples of biasing circuits. (4mrks)

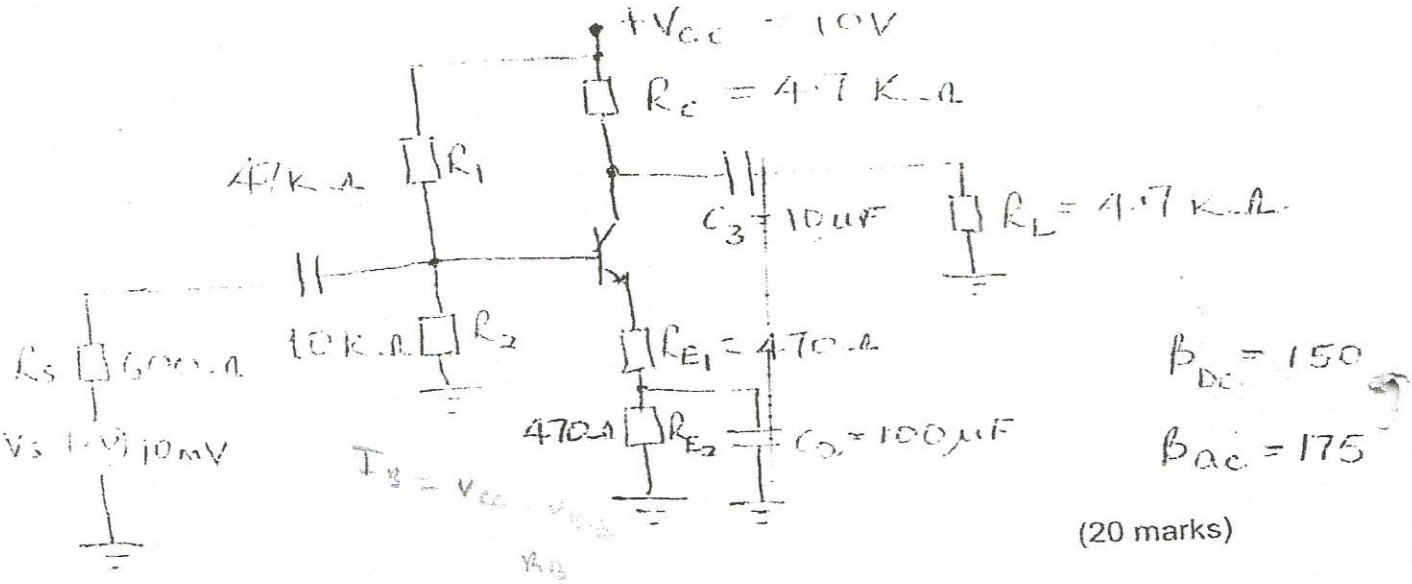
(iv) Determine Vc, Ve and VCE in the circuit given. Assume β_{DC} = 100 and VBE = 0.7V

Notice how the transistor is oriented in the diagram; with the positive emitter supply at the tope and the negative collector supply at the bottom. (PNP transistor) (3mrks)



6. For the amplifier in the following figure determine the total collector voltage and the total output voltage (dc and ac).

Draw the waveforms.
Divide your analysis into DC and AC analysis.



(20 marks)

(1mrk)

(7(i) Name the 3 terminals of a JFET.

(ii) Does an n-channel JFET require a positive or negative value for VGS. (1mrk)

(iii) How is drain current controlled in a JFET. (1mrk)

(iv) With the help of JFET drain characteristics describe and explain the 3 different operating regions of the n-channel JFET. (7mrks)

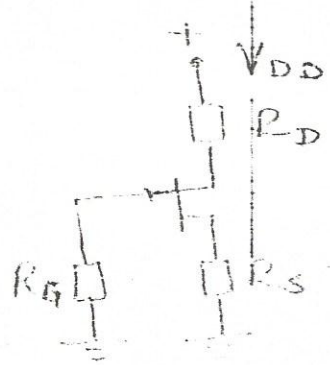
(v) Define and compare the terms pinch-off and cut-off voltage for an n-channel JFET. (3mrks)

(vi) It is often desirable to bias a JFET near the midpoint of its transfer characteristic curve where ID = IDSS/2 when VGS = VGS(off)/3.4 i.e

$$ID = IDSS\left[1 - \frac{VGS}{VGS\ (off)}\right]^2$$

[3 marks]

(vii) Select resistor values for R_D and R_s in figure below to set up an approximate midpoint bias. For the JFET shown, the parameters are IDSS = 12m A and VGS (off) = -3V, VD should be approximately 6V (one half of VDD). (4mrks)



$V_{DD} = 12V$

$R_G = 10M\Omega$

8(i) Name the 2 basic types of MOSFET'S. (1mrk)

Depletion mosfet DE-MOSFETS

Enhancement mosfet

(ii) If the gate-to-source voltage in a depletion MOSFET is zero what is the current from drain the source? (1mrk)

There will be current that will flow from the drain source.

(iii) Describe the operation of D-MOSFET and E MOSFET. Include in your answer exemplary transfer characteristics for each case. (6 mrks)

(iv) For a certain D-MOSFET, I_{DSS} = 10mA and $V_{GS(off)}$ = -8V

(I) Is this an n-channel or a p-channel P-Channel. (1mrk)

(II) Calculate ID at VGS = -3V (1mrk)

(III) Calculate ID at VGS = +3V (1mrks)

$I_D = 10mA\left(1 - \frac{-8}{-3}\right)^2$

$10 = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

$= 10mA\left(1 - \frac{-8}{3}\right)^2$

(v) The data sheet for a 2N7008 E-MOSFET gives ID(on) =500mA (minimum at VGS = 10V and VGS = IV. Determine the drain current for VGS = 5V. (2mrks)

(vi) Name various MOSFET bias circuits. Drain-feedback bias (3mrks)

Source, Drain, Gate. Voltage-divider bias

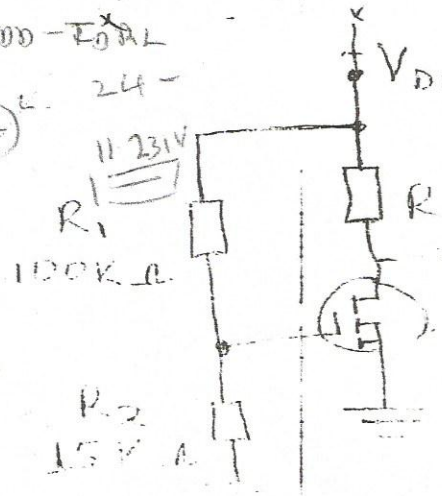
(vii) Determine VGS and VDS for the E_MOSFET circuit in figure below. Assume this particular MOSFET has minimum values $I_{D(on)}$ = 200mA at VGS = 4V and $V_{GS(th)}$ = 2V. (4mrks)

$V_{DS} = V_{DD} - I_D R_L$

$I_D = 0.05(3-2)^2$

$= 0.063A$

$= 63.8mA$



If $I_G = 0$, then $V_{DS} = \frac{1}{2}V_{DD}$

$= \frac{1}{2} \times 24$

$= 12V$

Voltage across R_2 =

$V_{GS} = \left(\frac{R_2}{(R_1+R_2)}\right) V_{DD}$

$V_{GS} = \frac{15}{100+15} \times 24$

$V_G = V_{DD} \times \frac{R_2}{R_1+R_2} = 24 \times \frac{15}{115} = 3.13V$

$V_{GS} = 10R_S$

$K = \frac{I_D}{(V_{GS} - V_{GS(th)})^2}$