

University Examinations 2012/2013

SECOND YEAR, SECOND SEMESTER, EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER TECHNOLOGY, COMPUTER SCIENCE AND BUSINESS INFORMATION TECHNOLOGY

ICS 2205: DIGITAL LOGIC

DATE: DECEMBER 2012

TIME: 2 HOURS

INSTRUCTIONS: Answer question one and any other two questions

QUESTION ONE – 30 MARKS

a.	With the aid of suitable diagrams, show how the NAND gate can be used to realize the other basic gates				
	(AND, NOT, OR AND NOR.	(6 Marks)			
b.	Distinguish between synchronous and asynchronous counters.	(4 Marks)			
c.	Implement a simple PLA circuit for the Boolean functions given below:	(8 Marks)			
	$F(A,B,C) = \Sigma m(0,2,4,6)$				
d.	What is the difference between a demultiplexer and a decorder?	(2 Marks)			
e.	In regards to flip flops, what is the race condition and how is it taken care of? (4 Marks)				
f.	Distinguish between synchronous and asynchronous inputs in flip flops. (3 Marks)				
g.	List three applications of flip flops. (3 Marks)				
QUESTION TWO – 20 MARKS					
a.	Simplify the given expressions.	(6 Marks)			
	i. $F = \overline{A} \ \overline{B} \ \overline{C} + \overline{A} \ B \ C + \overline{A}BC + AB\overline{A}$				
	ii. $F = XY + XZ + XYZ (XY + Z)$				
	iii.				
b.	Design and way demultiplexer and explain its operation.	(4 Marks)			
c.	Minimize the following logic function using k-maps and realize it using logic gates	(6 Marks)			
	$F(A,B,C,D) = \Sigma m(1,3,4,5,6,7,9,12,13)$	(6 Marks)			
d.	With the aid of a suitable diagram and truth table, explain the operation of a clocked RS flip flop.				

(4 Marks)

QUESTION THREE – 20 MARKS

a. The diagram shows a seven segment. Find the expression for the "b" segment, minimize it and implement it using logic gates. (10 Marks)

b. What is a half adder? With the aid of a truth table and a suitable diagram, explain how a 4 bit full adder works and explain how this 4-bit adder can be used as a substractor. (10 Marks)

QUESTION FOUR - 20 MARKS

a.	What are universal gates? Construct a logic circuit using NAND gates only for the expression.	
	$\mathbf{x} = \mathbf{A}, (\mathbf{B} + \mathbf{C})$	(8 Marks)
b.	Derive the expressions for a digital magnitude comparator capable of comparing two 4 –	bit numbers and
	give the three outputs $A = B$, $A > B$ and $A < B$	(6 Marks)
c.	ith the help of clocked SRflip flops and waveforms explain the working of a 4-bit SISO shift register.	
		(6 Marks)

QUESTION FIVE – 20 MARKS

a.	With	e bit binary ripple	
	down	counter.	(10 Marks)
b.	Draw	the circuit of a TTL NAND gate and explain its operation in brief.	(6 Marks)
c.	With	reference to logic families, define:	
	i.	Propagation delay	(2 Marks)
	ii.	Power consumption	(2 Marks)