MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY

P.O. Box 972-60200 – Meru-Kenya.
Tel: 020-2069349, 061-2309217. 064-30320 Cell phone: +254 712524293, +254 789151411
Fax: 064-30321
Website: www.mucst.ac.ke Email: info@mucst.ac.ke

University Examinations 2012/2013

SECOND YEAR, SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR
OF BUSINESS INFORMATION TECHNOLOGY
AND
SECOND YEAR, SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR
OF SCIENCE IN INFORMATION TECHNOLOGY

ICS 2205: DIGITAL LOGICS

DATE: APRIL 2013   **TIME: 2 HOURS**

INSTRUCTIONS: *Answer question **one** and any other **two** questions*

QUESTION ONE – 30 MARKS

a. With the aid of suitable diagram, show how the NOR gate can be used to realize the other basic gates (AND, NOT, OR and NAND)   (6 Marks)
b. Distinguish between synchronous and asynchronous counters.   (4 Marks)
c. Implement a simple PLA circuit for the Boolean function given below.   (8 Marks)

   $F(A,B,C) = \Sigma m(0,2,4,6)$

d. What is the difference between a multiplexer and an encoder?   (2 Marks)
e. List the advantages of a programmable logic device over fixed function ICs.   (3 Marks)
f. Distinguish between synchronous and asynchronous inputs in flip flops.   (3 Marks)
g. Design a 4 to-1 multiplexer and explain its operation.   (4 Marks)

QUESTION TWO – 20 MARKS

a. Simplify the given expressions.   (6 Marks)
   i. $F=C(B+C) (A+B+C)$
   ii. $F=XY+\overline{XY} + X\overline{Y}Z (XY+Z)$

b. Minimize the following logic function using K-maps and realize it using logic gates.
   $F(A,B,C,D)= \Sigma m(1,3,4,5,6,7,9,12,13)+ \Sigma d(0,2,8)$ (6 Marks)

c. With the help of a block schematic diagram and neat wave forms, explain a clocked J-K flip-flop that is triggered by the positive – going edge of the clock signal.   (8 Marks)

QUESTION THREE – 20 MARKS

a. Design a binary to gray code convertor. (10 Marks)
b. What is a half adder? With the aid of a truth table and a suitable diagram, explain how a 3-bit full adder works and explain how this 3-bit adder can be used as a subtractor. (10 Marks)

QUESTION FOUR – 20 MARKS

a. What are universal gates? Construct a logic circuit using NAND gates only for the expression X=A(B+C) (8 Marks)
b. Derive the expressions for a digital magnitude comparator capable of comparing two 3-bit numbers and give the three outputs A=B, A>B and A<B (6 Marks)
c. With the help of clocked SR flip flops and waveforms explain the working of a 4-bit SISO shift register. (6 Marks)

QUESTION FIVE – 20 MARKS

a. With the help of clocked JK flip flops and waveforms, explain the working of a three bit binary ripple up counter. (7 Marks)
b. Explain the following logic families and compare their performances. (7 Marks)
   i.   ECL
   ii. TTL
c. Reduce the following equation using K-map. (6 Marks)
   Y=A'B'C' + AC'D' + AB' + ABCD'+A'B'C