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University Examinations 2012/2013

FIRST YEAR, FIRST SEMESTER, EXAMINATION FOR THE DEGREE OF BACHELOR OF BUSINESS INFORMATION TECHNOLOGY AND BACHELOR OF SCIENCE IN COMPUTER SCIENCE

ICS 2101: COMPUTER ORGANIZATION

DATE: DECEMBER 2012 **TIME: 2 HOURS**

INSTRUCTIONS: *Answer question **one** and any other **two** questions*

QUESTION ONE – 30 MARKS

a. Show that:
(A + B) (A + C) = A + BC and ascertain the proof using **truth tables**. (6 Marks)
b. Using an appropriate diagram briefly discuss **memory hierarchy.** (4 Marks)
c. Express the following memory capacities in bytes:
   i. 2GB (1 Mark)
   ii. 0.5TB (1 Mark)
   iii. 500 Mega Bits (1 Mark)

d. Briefly explain the following:
   i. Programmed I/O (2 Marks)
   ii. I/O Processor (2 Marks)
e. Using an appropriate diagram, describe the instruction cycle. (3 Marks)
f. What do you understand by the term "bus" as used in computer systems? Identify the three types of system buses in the CPU and briefly describe each of them. (3 Marks)
g. By using circuits, symbols and truth tables, distinguish an AND gate from an OR gate. (4 Marks)
h. Given the infix expression Z⟵ (A*B) + (W*Y)
   i. Express the infix expression above in postfix notation; **hence** show the **stack operations** for the processing of the expression. (2 Marks)
   ii. Using **two address instruction set architecture;** use the requisite mnemonics to show the processing of the above infix expression. (2 Marks)

QUESTION TWO – 20 MARKS

a. Given the Boolean expression below:

AB + A(B+C) + B(B+C)

i. Simplify the Boolean expression to a **minimum** number of literals (4 Marks)
ii. Draw logic gate circuits for the initial expression and the simplified equivalent. (3 Marks)
iii. Use truth tables to proof that the two logic circuits are equivalent. (3 Marks)

b. Distinguish between **computer organization** and **computer architecture** and provide relevant applications of each. (2 Marks)
c. Briefly discuss the following:
i. Instruction pre-fetching (2 Marks)
ii. Pipelining (2 Marks)
iii. Memory address map (2 Marks)
iv. Program status word (2 Marks)

QUESTION THREE – 20 MARKS

a. Define the following addressing modes and give one example of each of them in assembly language.
i. Immediate addressing (2 Marks)
ii. Direct addressing (2 Marks)
b. Convert the following into reverse polish notation. (2 Marks)
A + B * (C*D +E* (F + G))

c. Explain any four instruction set design issues. (4 Marks)
d. Using a state diagram, explain the **instruction cycle** that has an **interrupt.** (6 Marks)
e. Explain the following terms:
i. Cache miss (1 Mark)
ii. Pipeline conflict (1 Mark)
iii. Delayed load (1 Mark)
iv. Virtual memory (1 Mark)

QUESTION FOUR – 20 MARKS

a. In order to compare different types of memories, their characteristics need to be considered, in this respect, discuss the characteristics given below:
   i. Access methods (2 Marks)
   ii. Performance (2 Marks)

b. With the aid of a diagram, describe the general structure of an I/O module and explain its functions. (5 Marks)

c. Explain stack and evaluate the following expression using stack: (3 +4)*[10(2 =6) + 8] (5 Marks)

d. A combinational logic structure is constructed from decision elements only. Using the requisite diagrams the functioning of the following:
   i. Decoder (4 Marks)
   ii. Multiplexer (4 Marks)

QUESTION FIVE – 20 MARKS

a. Describe the following methods of enhancing CPU performance:
   i. Hyper threading (4 Marks)
   ii. Dual core (4 Marks)

b. Describe the following CPU support chips:
   i. DMA (2 Marks)
   ii. Real Time Clock (RTC) (2 Marks)

c. Give an elaborate description of interrupt driven I/O. (4 Marks)

d. Draw a logical network that implements the following equations:
   i. Z = $\overline{(A + B)}$ (2 Marks)
   ii. Z = $\bar{A}.\bar{B}$ (2 Marks)