**SOUTH EASTERN KENYA UNIVERSITY**

**UNIVERSITY EXAMINATIONS 2016/2017**

**FIRST SEMESTER EXAMINATION FOR THE DEGREE OF**

**BACHELOR SCIENCE IN ELECTRONICS**

**ELC 404: INTEGRATED CIRCUIT DESIGN**

**7TH**

**DECEMBER, 2016**

**TIME:10.30-12.30 P.M**

**INSTRUCTIONS TO CANDIDATES**

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



**This paper consists of FIVE questions.**

**Answer question ONE and any other TWO questions.**

**Question ONE carries 30 mark while the other TWO questions carry 20**

**marks each**

**QUESTION 1, 30 MARKS [COMPULSORY]**

a) What is an Integrated circuit

b) Differentiate between direct and indirect band gap

[2 marks]

[4 marks]

c) State two reasons why GaAS is used in many applications such as microwaves and ICs

[2 marks]

d) What is a charged coupled device (CCD)

[2 mark]

e) A particular layer of MOS circuit has resistivity of 10 Ohms-cm. the section is 55 μm long,

5 μm wide and 1 μm thick. Calculate

i.

ii.

Sheet resistance

Resistance of the layer

[ 3 marks]

[ 2 marks]

f) State tree advantages of using static CMOS

g) Compare IC based on MOS and bipolar transistor technologies

h) Draw the circuitry representation of I2L inverter

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[3 marks]

[3 marks]

[2 marks]

Page 1

i) Describe three general functions of computer register

j) Draw a CMOS schematic diagram implementation of D-latch

**QUESTION 2 [20 MARKS]**

a) Explain the functions of the following registers

[ 3 marks]

[4 marks]

i.

ii.

iii.

iv.

Memory address register

Program counter

Accumulator register

Memory data register

[2 marks]

[2 marks]

[2 marks]

[2 marks]

b) Describe the two types of charged coupled devices

c) Draw the logic operations- NAND gate and its truth table

[8 marks]

[4 marks]

**QUESTION 3, [20 MARKS]**

a) State two main factors considered during design of any basic circuit [ 2 marks]

b) State two models used by IC designers to shrink the size of a circuit

c) Define the following terminologies used in ICs designs

[2 marks]

i.

ii.

iii.

iv.

Epitaxy

Wafer

Metallization

Bonding

[1 mark]

[1 mark]

[1 mark]

[ 1 mark]

d) Using a physical structure of p-Si substrate with a thin film layer of SiO2 describe

the process of photolithography

**QUESTION 4, [20 MARKS]**

a) State three advantages of using dynamic CMOS

b) Draw a CMOS inverter circuit and its transfer characteristics

[12 marks]

[3 marks]

[5 marks]

c) State and explain three circuit elements used in CMOS and radio frequency design

[6 marks]

d) Draw the physical structure of BiMOS npn transistor

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[6 marks]

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**QUESTION 5, [20 MARKS]**

a) The figure 1 below shows a DTL circuit model with high inputs. Use it to attempts

questions that follow. Given that β = 40, in the diagram 5K=5kῼ and 2.2K=2.2kῼ,

+5=+5V, 0.7=0.7V, 0.2=0.2V and 0.8=0.8V

Given that all the outputs are high and all the system is saturated. Find

i.

ii.

iii.

iv.

The voltage at point P

The current I1

The current I2

The current IB

[2 marks]

[ 1 marks]

[ 1 marks]

[2 marks]

v.

Calculate the maximum collector current when the transistor is saturated [2 marks]

vi.

vii.

The current I3

The maximum load current, Vin and Iin

[2 marks]

[3 marks]

b) Using inverters, and gates and OR gates implement a 5 X 8 X 4 (V\*P\*Z)

programmable logic array with following outcomes

*z*1 *ab d e* *a b c de* *bc* *de*

*z* 2 *a c e*

*z* 3 *bc* *de* *c de* *bd*

*z* 4 *a c e* *ce*

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[7 marks]

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