

MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY

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University Examinations 2013/2014

FIRST YEAR, SECOND SEMESTER, EXAMINATION FOR THE DEGREE OF BACHELOR OF MATHEMATICS AND COMPUTER SCIENCE

ICS 2101: COMPUTER ORGANIZATION

TIME: 2 HOURS DATE: APRIL 2014 **INSTRUCTIONS:** Answer question **one** and any other **two** questions **QUESTION ONE (30 MARKS)** With a block diagram, explain the organization of a control unit. a) (6 marks) b) Distinguish between computer architecture and computer organization giving examples. (6 marks) c) Define the term interrupt. Explain various types of Interrupts in detail. (6 marks) d) Explain the performance effect of bus width to a computer system. (6 marks) e) Discuss the concept of virtual memory. (6 marks) **QUESTION TWO (20 MARKS)** a) Discuss two hard disk interface standards. (5 marks) Briefly explain Von-Neumann architecture for computers. (5 marks) b) c) Explain major characteristics of PCI bus. (5 marks) d) Define pipelining? Explain instruction pipelining in detail. (5 marks) **QUESTION THREE (20 MARKS)** Explain the cache memory. (1 mark) a) Draw memory hierarchy and explain all types of memory. b) (5marks)

c)	Differentiate between programmed i/0 and interrupt driven I/O and state how each affects	
	the performance.	(5 marks)
d)	Write short notes on the following:	
	i. Parallel processing	(3 marks)
	ii. Compilers	(3 marks)
	iii. Interpreters	(3 marks)
QU	JESTION FOUR (20 MARKS)	
a)	What are the causes of system complexity in CISC architecture?	(4 marks)
b)	How is paging different from segmentation in memories?	(2 marks)
c)	With the aid of a diagram, explain the need and the process by which the physical address	
	changes to logical address and vice-versa.	(5 marks)
d)	Compare and contrast different types of associative memories.	(5 marks)
e)	Explain the following:	
	i. CMOS	(4 marks)
	ii. POST	(2 marks)
QU.	ESTION FIVE (20 MARKS)	
a.	Convert octal number 327 to decimal.	(2 marks)
b.	Explain the basic concept of RAID and its potential contribution to reliabilit	•
	performance.	(3 marks)
c.	Analyse DMA operation in regard to data transfer in an I/O module.	(5 marks)
d.	Discuss software polling and bus arbitration as methods of servicing interrup	ots. (5 marks)
e.	Explain the error detection and correction in memory using parity bits techn	ique. (5 marks)