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University Examinations 2012/2013

FIRST YEAR, SECOND SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN MATHEMATICS AND PHYSICS AND BACHELOR OF SCIENCE IN MATHEMATICS AND COMPUTER SCIENCE
AND
FIRST YEAR, FIRST SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF BUSINESS IN BUSINESS INFORMATION TECHNOLOGY

ICS 2101: COMPUTER ORGANIZATION

DATE: APRIL 2013 **TIME: 2 HOURS**

INSTRUCTIONS: *Answer question* ***one*** *and any other* ***two*** *questions*

QUESTION ONE – 30 MARKS

a. Show that:
$(x + y)(x + z) = x + yz$ and ascertain the proof using truth tables. (4 Marks)
b. Explain the characteristics of RISC and CISC (4 Marks)
c. Convert the following to binary (3 Marks)
   i. 453_{10}
   ii. $1C5_{16}$
   iii. 56_8

d. Give short notes on the following types of computer memory and their application.
   i. I/O Ports (2 Marks)
   ii. Flags (2 Marks)
   iii. Buffer (2 Marks)
e. Using two's complement, perform the following arithmetic operation

$777_8 - 25_{10}$ (give your answer as an hexadecimal)

f. Using a state diagram, explain the instruction cycle. (4 Marks)
g. Draw a clear distinction between the following:
   i. Computer architecture and computer organization. (2 Marks)
   ii. Fixed point representation and floating point representation. (2 Marks)
   iii. One address instruction and a three address instruction. (2 Marks)

QUESTION TWO – 20 MARKS

a. Given the statement Y=(A-B)/(C+D*E), illustrate its solution using:
   i. A three address instruction (2 Marks)
   ii. A two address instruction (2 Marks)
   iii. A one address instruction (2 Marks)

b. Analyse how the diverse I/O devices are interfaced to computer CPU and buses for the following methods: (8 Marks)
   i. Programmed I/O
   ii. Interrupt – driven I/O
   iii. DMA
   iv. I/O processor

c. Clearly describe the hierarchical memory organization. (4 Marks)

d. With a suitable example differentiate between big endianess and little endianess. (2 Marks)

QUESTION THREE – 20 MARKS

a. "Computers are crucial pillars for Kenya to achieve vision 2030". Qualify this assertion putting into consideration the advancements made in ICT since the third generation of computers. (8 Marks)

b. Define the term register in the context of CPU. Identify any five registers (in this context), with their corresponding functions. (6 Marks)

c. Differentiate between:
   i. SRAM and DRAM (2 Marks)
   ii. SDRAM and DDR SDRAM (2 Marks)
   iii. EPROM and EEPROM (2 Marks)

QUESTION FOUR – 20 MARKS

a. Given the Boolean expression below:
   AB + A (B + C) + B (B + C)

   i. **Simplify** the Boolean expression to a **minimum** number of literals. (3 Marks)
   ii. Draw logic gate circuits for the initial expression and the simplified equivalent. (2 Marks)
   iii. Use truth table to proof that the two logic circuits are equivalent. (3 Marks)

b. Express the following memory capacities in Kilobytes.
   i. 2GB (1 Mark)
   ii. 0.5TB (1 Mark)
   iii. 400 Megabits (1 Mark)
   iv. 6400 bits (1 Mark)

c. Briefly discuss what you understand by the term bus arbitration. With an example explain two classes of bus arbitration schemes. (3 Marks)

d. Using an appropriate illustrative diagram explain the internal components and basic organization of the CPU. Outline the function of each of the major components. (5 Marks)

QUESTION FIVE – 20 MARKS

a. In the context of cached memory system explain the performance factors hit ratio and miss penalty. Explain also the principle of locality and its relevance to cached memory performance. (5 Marks)

b. Virtually all computers provide a mechanism in which I/O modules or memory might interrupt normal CPU operation. Using a diagram explain interrupt cycle in this context. (5 Marks)

c. Draw a logical network that implements the following equations:
   i. $Z=\overline{(A + B)}$ (2 Marks)
   ii. $X=(A + B) * (\bar{A}. + \bar{B})$ (2 Marks)

d. Define the following addressing modes and give an example illustrating implementation of each case.
   i. Register addressing (2 Marks)
   ii. Implied addressing (2 Marks)
   iii. Indirect register addressing (2 Marks)