MASENO UNIVERSITY

UNIVERSITY EXAMINATIONS 2016/2017

FOURTH YEAR FIRST SEMESTER EXAMINATION FOR DEGREE OF BACHELOR OF SCIENCE IN PHYSICS AND MATERIALS SCIENCE WITH INFORMATION TECHNOLOGY

MAIN CAMPUS

SPH 406: DIGITAL ELECTRONICS II

Date: 12th December, 2016 Time: 12.00 - 3.00pm

INSTRUCTIONS:

- Answer Question ONE in Section A and any other TWO in Section B.

INSTRUCTIONS: Question 1 of section A is **COMPULSORY.**

Attempt **ANY TWO** questions from section B.

SECTION A: This section is **COMPULSORY.**

1. a) (i) State commonly used display techniques. **(2 marks)**
(ii) Give four important criteria for choosing a display technique. **(4 marks)**

b) A logic circuit in figure 1 is two-bit binary counter where B0 is the LSB.

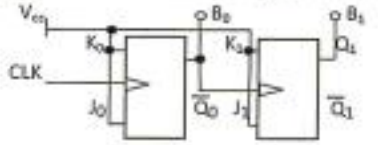

Fig. 1

The counter is negative-edge triggered and is initially cleared.
(i) Draw a *truth table* for the output B_0B_1 for the first five clock pulses. **(2 marks)**
(ii) What type of counter is figure 3? **(1 marks)**
(iii) What is the modulus of the counter? **(1 mark)**
(iv) Although the input logic in simple JK flip-flop eliminates some of the timing problems inherent in RS flip-flop, its final state still may not be determined when J=K =1.
Explain. **(2 marks)**

c) (i) What is a register? **(1 mark)**
(ii) What are the basic functions of a register? **(2 mark)**
(iii) Name any two shift registers. **(2 marks)**

d) (i) Define a *circuit buffer*. **(2 marks)**
(ii) Cite any three properties of an ideal *voltage buffer*. **(3 marks)**
(iii) Draw a schematic diagram of a *unity gain buffer amplifier*. **(2 marks)**

e) (i) Define a *voltage comparator*. **(2 mark)**
(ii) Draw a schematic diagram of a voltage comparator with a fixed voltage divider reference source and give an equation that relates V_{ref} to V_{cc}. **(4 marks)**

SECTION B: Answer **ANY TWO** questions.

Each question carries twenty (20) marks.

2. a) Define a Schmitt trigger and give its symbol. **(4 marks)**

b) There are many ways of implementing Schmitt trigger. Draw one that uses a non-inverting op-amp and explain how it works. **(13 marks)**

(iii) The diagram in figure 2 shows a signal into a Schmitt trigger. Draw the corresponding signal from the output of the trigger (i.e V_o). **(3 marks)**

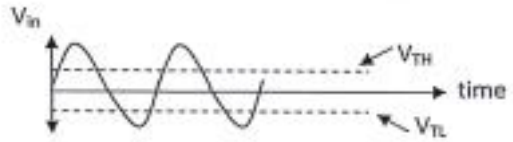

Fig. 2

3. a) (i) What is a *pulse width* of a monostable? **(1 mark)**

(ii) Cite components that are used to control pulse width. **(2 marks)**

(iii) What parameter determines the duration of the pulse width? **(2 marks)**

b) Define an *astable multivibrator*. **(1 mark)**

c) (i) Explain what is meant by the *delay mode* operation of a 555 timer. **(1 mark)**

(ii) I) Find the pulse width of for a 555 timer in a monostable operation if $R_A = 910\Omega$ and $C = 0.1\mu F$. **(4 marks)**

II) If $V_{CC} = 5V$, find the threshold (V_{Thres}) and trigger (V_{Trig}) voltages. **[3 marks]**

III) Given the input waveform in figure 3, draw to scale the output voltage waveform and the voltage across the timing capacitor. (Indicate the V_{Thres}, V_{Trig} and output pulse width) **(6 marks)**

Fig. 3

4. a) The diagram in figure 4 shows an electronic circuit.

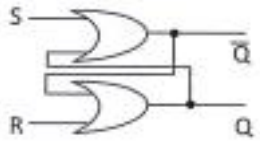

Fig. 4

(i) Name the circuit. **(1 mark)**

(ii) Draw the *Truth table* of the circuit and state what each output describes. **(4 marks)**

(iii) Explain the limitation of this circuit. **(5 marks)**

(iv) On its own, where is this circuit applied in life?
Draw a schematic diagram of this application. **(5 marks)**

b) (i) Define a *flip-flop*. **[1 mark]**
(ii) Is a flip-flop a *combinational logic* and *a sequential logic*? **[1 marks]**
(iii) Explain the difference between the logics in (ii) above **[3 marks]**

5. a) (i) Draw a schematic diagram of an *asynchronous 3-bit D-type* counter wired in a toggling mode. **(6 marks)**
(ii) Why is it called *asynchronous*? **(2 marks)**
(iii) (iii) Determine the output wave Q_1 for the counter in (i) above using the waveforms in figure 5. Q_1 is initially LOW. **[4 marks]**

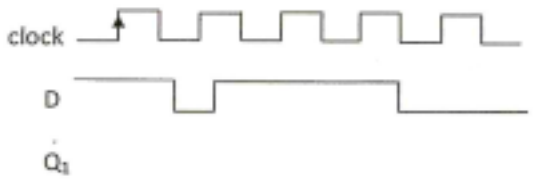

Fig.5

b) (i) Cite two advantages that a *synchronous counter* has over *asynchronous counter*. **(2 marks)**
(ii) Draw a BCD version of the counter in (a) above. **(6 marks)**

END