**MERU UNIVERSITY OF SCIENCE AND TECHNOLOGY**

**P.O. Box 972-60200 – Meru-Kenya**

**Tel: 020-2069349, 061-2309217. 064-30320 Cell phone: +254 712524293, +254 789151411**

**Fax: 064-30321**

**Website:** [**www.must.ac.ke**](http://www.must.ac.ke) **Email:** **info@must.ac.ke**

**University Examinations 2016/2017**

 THIRD YEAR, FIRST SEMESTER EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER TECHNOLOGY

**SPS 3300: BASIC ELECTRONIC CIRCUITS ANALYSIS & DESIGN**

**DATE: December, 2016 TIME: HOURS**

**INSTRUCTIONS:** *Answer questions* ***one*** *and any other* ***two*** *questions.*

**QUESTION ONE - (30 MARKS)**

1. Convert  to binary. (2 Marks)
2. Subtract  from  using basic rules of binary subtraction(2 Marks)
3. The figure below shows a logic gate
4. Present the truth table for the gate. (2 Marks)
5. Show how the same results can be realized using NOT, AND and OR gates

(2 Marks)

1. Differentiate between weighted and unweighted codes. (2 Marks)
2. Simplify the truth table below using Karnaugh maps. (2 Marks)

|  |  |  |
| --- | --- | --- |
| A | B | Y |
| 0011 | 0101 | 0111 |

1. Distinguish between UVPROM and EEPROM (2 Marks)
2. Design a circuit to implement the function below using logic gates. (3 Marks)

$$Y=AB+AC^{'}$$

1. Convert the following binary to gray code  (2 Marks)
2. Using a diagram explain the term parallel input-serial output register. (2 Marks)
3. What are the salient features of ASCII code. (2 Marks)
4. Simplify using Boolean algebra. (3 Marks)

$y=AB+ A^{'}$B $( AB)^{'}$

1. Perform $\left(07FA\right)\_{16}+ \left(02AB\right)\_{16}$ (2 Marks)
2. Explain the term canonical form of Boolean expression. (2 Marks)

**QUESTION TWO (20 MARKS)**

1. Transform the following sum of product to product of sums. (3 Marks)

 $z=AB+ (A^{'}B^{'})^{'}$

1. (i) Present the truth table for a half-adder. (2 Marks)

(ii) Express the outputs of the half-adder in Boolean form. (2 Marks)

1. Design a circuit using logic gates to implement the half-adder. (3 Marks)
2. Differentiate between a combinational logic circuit and a sequential logic circuit(2 Marks)
3. Find the expanded form of the following Boolean expressions.
4.  (2 Marks)
5.  (2 Marks)
6. For a Boolean function  show that  (4 Marks)

**QUESTION THREE (20 MARKS)**

1. Briefly describe the features of EBCDIC code. (3 Marks)
2. What is a multiplexer? (2 Marks)
3. (i) Present the truth table of a 4:1 multiplexer. (2 Marks)

(ii) Implement a 4:1 multiplexer circuit using AND OR and NOT gates. (4 Marks)

1. Use Karnaugh maps to minimize the following Boolean expression.

$Z=\overbar{A}\overbar{B}\overbar{C}\overbar{D}$ + $\overbar{A}\overbar{B}C\overbar{D}$ +$\overbar{A}B\overbar{C}$ D + $\overbar{A}$ BCD + A$\overbar{B}\overbar{C}\overbar{D}$ + A$\overbar{B}$C$\overbar{D}$+ AB$\overbar{C}$D + ABCD(6 Marks)

1. (i) Using a block diagram explain the working of a 2 – 4 decoder. (2 Marks)

(ii) Draw the truth table for the 2 – 4 decoder. (1 Mark)

**QUESTION FOUR (20 MARKS)**

1. Convert  excess 3 code. (2 Marks)
2. Using a truth table and a logic circuit explain the working of R-S flip flop. (6 Marks)
3. Use Mc Chisky tabuler method to minimize  (6 Marks)
4. Write down the Boolean expression implemented by the circuit below; (3 Marks)
5. Use the $I^{'}s$ compliment to perform  (3 Marks)