MASENO UNIVERSITY

UNIVERSITY EXAMINATIONS 2013/2014

FIRST YEAR FIRST SEMESTER EXAMINATIONS FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE & TECHNOLOGY

(MAIN CAMPUS)

SCS 104: ELECTRONICS

Date: 29th November, 2013 *Time: 11.00 a.m. - 1.00 p.m.*

INSTRUCTIONS:

a) Attempt Question ONE and any other TWO complete questions.

b) Diagrams, where necessary should be clearly drawn and labeled.

Q1 (a) (I) What is a semiconductor element? 1 mark

(ii) State the factors that influence electrical conductivity in semiconductor materials; and differentiate between intrinsic and extrinsic conductivities as applied to semiconductors.

5 marks

(iii) Explain, giving relevant sketches, the formation of either p-type or n-type material.

5 marks

(iv) Determine the number of density atoms which has to be added to an intrinsic Ge semiconductor to produce an n-type material of conductivity 5 Siemens/cm given that the mobility of electrons in the n-type material is 3850 cm2/volt sec. Take electric charge, $\mathbf{e = 1.60 \times 10^{-19}}$ Coulombs.

5 marks

(b) (i) Explain the essence of transistor biasing.

2 marks

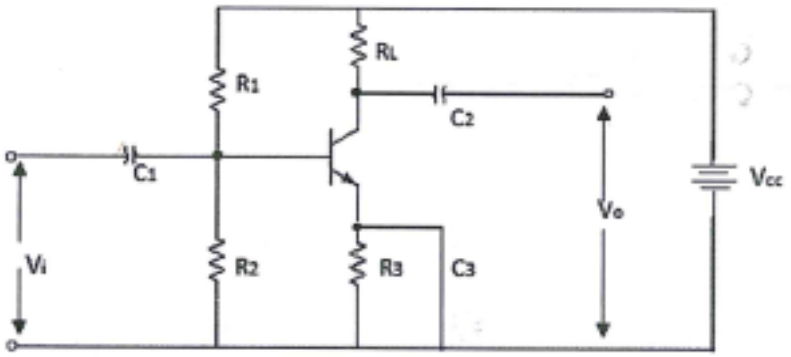
(ii) State the factors that affect the operation / or performance of a transistor amplifier; and give the classification of the amplifiers based on one of the factors that you have stated.

5 marks

(iii) State <u>one</u> structural and <u>one</u> operational difference between FETs and Bipolar transistors.

2 marks

(c) The circuit drawn below is that of a self-bias transistor amplifier circuit.



Explain the function of C_1, C_2, C_3, R_1 and R_2

5 Marks

6

SECTION II

Answer any Two complete questions from this section

Q2. (a) Explain:

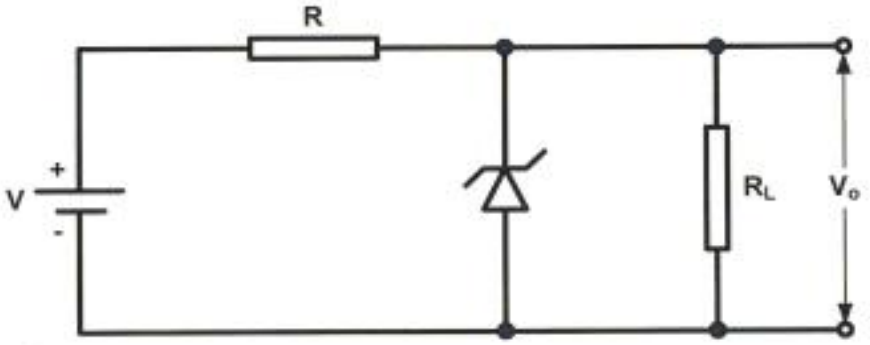
(i) The occurrence of avalanche and zener breakdowns in p-n junction.

4 marks

(ii) The operations and at least one application of photo diode.

4 marks

(b) The circuit drawn below depicts a typical application of a zener diode.



Assume that the supply voltage, v_s is 9 volts, and that the zener voltage, $V_z = V_o = 6$ V If the maximum zener current that can safely flow is 20 mA.

i) Determine the value of the series resistance, R

3 marks

ii) If the load resistance, R_L of 1 KΩ is connected across the zener diode, calculate the load current, I_L, and the zener current, I_z.

4 marks

iii) Calculate the maximum value of R_L that can be used.

3 marks

iv) Explain the role of zener diode in this circuit.

2 marks

Q3. (a) Draw and clearly label the a.c equivalent circuit of a transistor amplifier using h- parameters; and explain the significance of each parameter.

6 marks

(b) The h- parameters of a transistor used as an amplifier in common emitter(CE) configuration are:

$h_{ie} = 800\ \Omega$, $h_{fe} = 46$, hoe $= 80 \times 10^{-6}$ Siemens, and hre $= 5.4 \times 10^{-4}$

If the load resistance is 5 KΩ and the effective source resistance is 500Ω,

Calculate the:

(i) Current gain — 4 marks

(ii) Input resistance — 4 marks

(iii) Voltage gain — 4 marks

(iv) Power gain, in dB — 2 marks

Q4 (a) What is wave rectification, and what is / are its essence in power supply?

4 marks

(b) (i) Draw a complete power supply circuit, and explain the operations of each component / block.

10 Marks

(ii) Sketch the expected waveform(s) at the output of every stage.

4 marks

(iii) Explain the major challenge(s) of using centre-tap transformer at the rectification stage.

2 Marks

3

Q5 (a) State the difference(s) between:

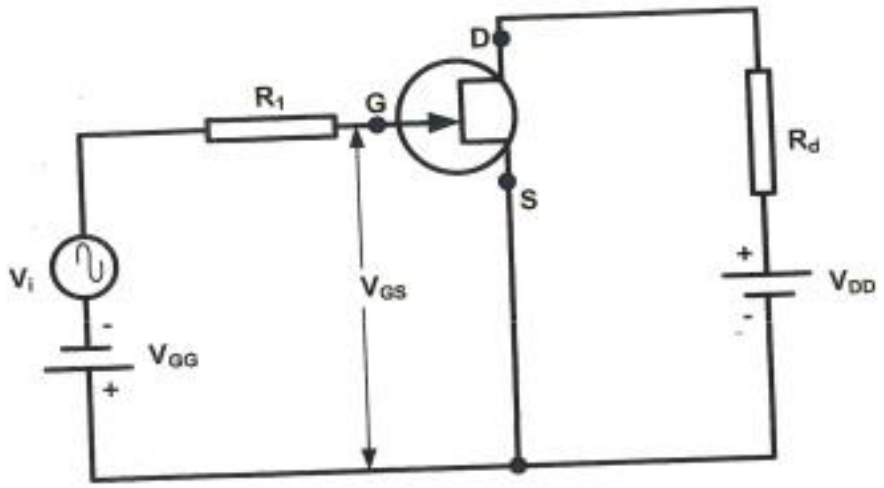
(i) JFET and MOSFET — 2 marks

(ii) N-channel and P-channel FET. — 2 marks

(b) Draw the structural diagram of a P-channel enhancement MOSFET and explain its operation. Sketch the expected current-voltage curves.

8 marks

(c) The circuit diagram below is that of FET amplifier with a gate-bias voltage, V_{GG}.



The operating parameters are: I_{DSS} = 10 mA, V_p { = V_{GS} (off)} = - 3V, V_{DD} = 25 V, I_D = 5 mA, and VDS = 5 V, determine:

(i) V_{GG} and R_D, state any assumption made. 5 marks

(ii) The voltage gain in dB. 5 marks