COMPUTER ORGANISATIN AND ARTITECTURE (BBIT 112) (CISY 111) 3rd trimester 2013

**KENYA METHODIST UNIVERSITY**

**END OF 3'***RD '***TRIMESTER 2013 (PT) EXAMINATION**

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| **FACULTY** |  | : | COMPUTING & INFORMATICS | | | | | | |
| **DEPARTMENT** | : | COMPUTER SCIENCE AND BUSINESS |  |  |  |  |  |  | INFORMATION |
| **UNIT CODE** |  | : | BBIT 112/CISY 111 | | | | | | |
| **UNIT TITLE** | | | | | | | | : | COMPUTER ORGANISATION AND ARCHITECTURE |
| **TIME** |  |  | : | 2 HOURS | | | | | |

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***Instructions:***

**SECTION A: Compulsory**

**Question One**

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| * Describe the following structures components of compute systems. State their functions and how they are organized. |  |  |  | (12mks) |

* C.P.U
* I/O Devices
* Memory
* Interconnection structure.

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| * Analyse the basic instruction cycle with provision of interrupts. Describe the steps of fetch-execute cycle and interrupt cycle. | |  |  | (8mks) |
| * What are the limitation of Bus performance. State two. | | |  | (4mks) |
| * Describe the following in the context of bus. |  |  |  | (6mks) |

* Bus arbitration
* Timing

**SECTION B: Answer any two questions from this section**

**Question Two**

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| * Provide a reason why peripherals cannot be connected directly to system bus. |  |  |  |  |  |  |  |  |  | (3mks) |
| * Describe the following I/O functionality. | | | | | | |  |  |  | (6mks) |

* Control al timing
* CPU communication
* Data buffering

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| * Describe the concept of direct memory access as a solution to input/output challenges. |  |  |  |  |  |  |  |  | (5mks) |
| * Explain the three categories of I/O devices. | | | | | |  |  |  | (6mks) |

**Question Three**

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| * Explain the role of the following memories. |  |  |  | (6mks) |

* Main memory
* Cache memory
* Virtual memory
* Explain the following memory access method and give examples. (8mks)
* Sequential
* Direct
* Random
* Associative

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| * The information stored in n level memory hierarchy, M1 to Mn, should satisfy the three important properties inclusion, coherence and locality. Explain the three properties. |  |  |  |  |  | (6mks) |

**Question Four**

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| * Describe the structure of hard disk in terms of cylinders, tracks, sectors and R/W heads. |  |  |  |  |  |  |  | (6mks) |
| * Describe the functions of the following CPU components. | | | | | | |  | (8mks) |

* Arithmetic and logic unit
* Control unit
* Register
* Internal bus

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| * Using FLYnn taxonomy describe the three main classes of parallel process. |  |  |  |  |  |  |  |  |  |  |  | (6mks) |

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