SOUTH EASTERN KENYA UNIVERSITY

UNIVERSITY EXAMINATIONS 2016/2017

FIRST SEMESTER EXAMINATION FOR THE DEGREE OF

BACHELOR SCIENCE IN ELECTRONICS

ELC 404: INTEGRATED CIRCUIT DESIGN

7TH DECEMBER, 2016 **TIME:10.30-12.30 P.M**

INSTRUCTIONS TO CANDIDATES

- **This paper consists of FIVE questions.**
- **Answer question ONE and any other TWO questions.**
- **Question ONE carries 30 mark while the other TWO questions carry 20 marks each**

QUESTION 1, 30 MARKS [COMPULSORY]

a) What is an Integrated circuit [2 marks]

b) Differentiate between direct and indirect band gap [4 marks]

c) State two reasons why GaAS is used in many applications such as microwaves and ICs [2 marks]

d) What is a charged coupled device (CCD) [2 mark]

e) A particular layer of MOS circuit has resistivity of 10 Ohms-cm. the section is 55 μm long, 5 μm wide and 1 μm thick. Calculate

i. Sheet resistance [3 marks]

ii. Resistance of the layer [2 marks]

f) State tree advantages of using static CMOS [3 marks]

g) Compare IC based on MOS and bipolar transistor technologies [3 marks]

h) Draw the circuitry representation of I^2L inverter [2 marks]

i) Describe three general functions of computer register [3 marks]

j) Draw a CMOS schematic diagram implementation of D-latch [4 marks]

QUESTION 2 [20 MARKS]

a) Explain the functions of the following registers

i. Memory address register [2 marks]

ii. Program counter [2 marks]

iii. Accumulator register [2 marks]

iv. Memory data register [2 marks]

b) Describe the two types of charged coupled devices [8 marks]

c) Draw the logic operations- NAND gate and its truth table [4 marks]

QUESTION 3, [20 MARKS]

a) State two main factors considered during design of any basic circuit [2 marks]

b) State two models used by IC designers to shrink the size of a circuit [2 marks]

c) Define the following terminologies used in ICs designs

i. Epitaxy [1 mark]

ii. Wafer [1 mark]

iii. Metallization [1 mark]

iv. Bonding [1 mark]

d) Using a physical structure of p-Si substrate with a thin film layer of SiO_2 describe the process of photolithography [12 marks]

QUESTION 4, [20 MARKS]

a) State three advantages of using dynamic CMOS [3 marks]

b) Draw a CMOS inverter circuit and its transfer characteristics [5 marks]

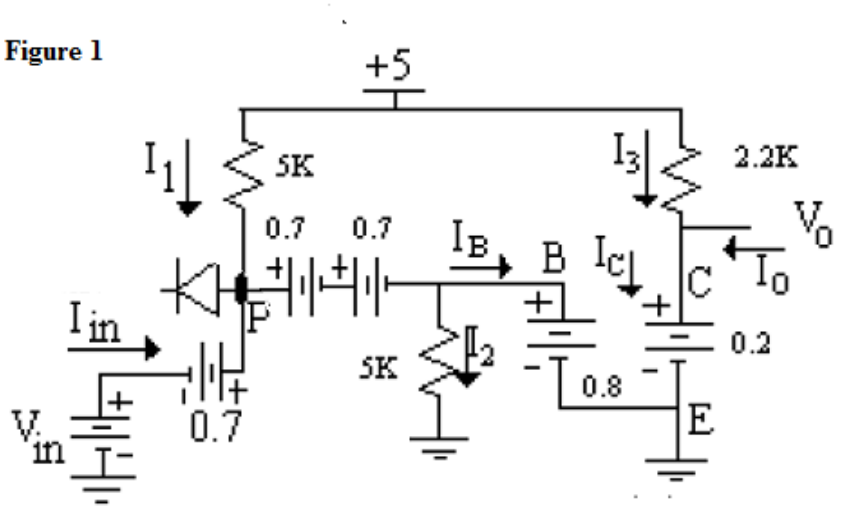
c) State and explain three circuit elements used in CMOS and radio frequency design [6 marks]

d) Draw the physical structure of BiMOS npn transistor [6 marks]

QUESTION 5, [20 MARKS]

a) The figure 1 below shows a DTL circuit model with high inputs. Use it to attempts questions that follow. Given that β = 40, in the diagram 5K=5kΩ and 2.2K=2.2kΩ, +5=+5V, 0.7=0.7V, 0.2=0.2V and 0.8=0.8V

Figure 1



Given that all the outputs are high and all the system is saturated. Find

i. The voltage at point P [2 marks]

ii. The current I_1 [1 marks]

iii. The current I_2 [1 marks]

iv. The current I_B [2 marks]

v. Calculate the maximum collector current when the transistor is saturated [2 marks]

vi. The current I_3 [2 marks]

vii. The maximum load current, V_{in} and I_{in} [3 marks]

b) Using inverters, and gates and OR gates implement a 5 X 8 X 4 (V*P*Z) programmable logic array with following outcomes [7 marks]

$$z_1 = a\bar{b}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bc + de$$
$$z_2 = \bar{a}\bar{c}e$$
$$z_3 = bc + de + \bar{c}\bar{d}\bar{e} + bd$$
$$z_4 = \bar{a}\bar{c}e + ce$$