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**University Examinations 2015/2016**

SECOND YEAR SECOND SEMESTER EXAMINATION FOR DIPLOMA IN ELECTRICAL ENGINEERING

**EEE 2254: DIGITAL ELECTRONICS II**

 **DATE: NOVEMBER 2015 TIME: 11/2 HOURS**

**INSTRUCTIONS:** *Answer question* ***one*** *and any other* ***two*** *questions*

**QUESTION ONE (30 MARKS)**

1. Define the two demorgan’s theorems. (4 Marks)
2. List three types of logic families currently in existence. (3 Marks)
3. Outline the following:
4. Flip-flop. (2 Marks)
5. Synchronous. (2 Marks)
6. Asynchronous. (2 Marks)
7. List three classes of registers using edge-triggered Dor J-K flip-flop. (3 Marks)
8. Simplify using Boolean expression

 (4 Marks)

1. Realize or implement the following Boolean expression using basic gates
2. Y=AB+CD+EF (2 Marks)
3. ABC+DEF using NAND gates only. (2 Marks)
4. Minimize the Boolean function using Karnaugh map

 (4 Marks)

**QUESTION TWO (15 MARKS)**

1. Briefly explain the characters of the following terms which constitute the logic families:
2. Fan-in (2 Marks)
3. Noise immunity. (2 Marks)
4. Power dissipation (2 Marks)
5. With aid of circuit diagrams explain briefly the difference in circuits operation of T.T.L and C MOS. (6 Marks)
6. State limitations of ripple counters. (3 Marks)

 **QUESTION THREE (15 MARKS)**

1. Define multipleker. (4 Marks)
2. Digital logic circuits are implemented using gates. The resultant circuits may posses their own symbol sketch a 4-line to 1-line multiplexer
3. Using the gate implementation.
4. Symbol.
5. Truth-table (12 Marks)

**QUESTION FOUR (15 MARKS)**

1. Compare briefly synchronous and asynchronous counters. (4 Marks)
2. Two warring factions A and B are to be reconciled by two friendly parties C and D. Given that for negotiations to take place A and B and either C or D must be present.
3. Draw the truth table that satisfies the given conditions. (3 Marks)
4. Draw the Karnaugh map from the truth table. (2 Marks)
5. Determine the Karnaugh minimum switching formula. (2 Marks)
6. Implement the switching formula (iv) above. (2 Marks)
7. Express the switching formula to NAND gates only. (2 Marks)